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A D-Band Low-Noise-Amplifier in SiGe BiCMOS with Broadband Multi-Resonance Matching Networks

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***Abstract* — Silicon amplifiers in D-Band are required to operate at high gain-bandwidth products and close to the cutoff frequency f_{max}. Multi-stage amplifiers commonly employ stagger-tuning to meet the desired bandwidth, but with sub-optimal noise and linearity. Better performance is achieved with broadband inter-stage matching and gain progressively distributed among the stages. This work proposes a design flow for broadband matching networks approximating the response of a doubly-tuned transformer. The technique is applied to design a 3-stage D-band LNA in BiCMOS 55 nm technology. Measurements show 28 dB gain, 127-168 GHz bandwidth, NF down to 5.2 dB and $>$ 2dBm output compression point with 30 mA DC current from 2V supply. The performance compare favorably against previous works.**

***Keywords* — D-band, BiCMOS, matching network, Low Noise Amplifier**

I. Introduction

The ever-increasing demand for portable data-intensive applications pushes the wireless network infrastructure to support communications with data rates in the order of 100 Gbps. High-capacity wireless links are gaining interest over optical fibers, especially in high-density urban environments, enabling flexible configurations and lower deployment cost. In this framework, mmWave and sub-THz bands are attractive, offering wide usable spectrum portions [1]. One of the major difficulties in the design of amplifiers for such kind of applications is the ability to provide enough gain over a very broad bandwidth, setting challenging demands on the gain-bandwidth product, typically in the order of several hundreds of GHz [2][3]. Given the low available gain of transistors, pushed close to the technology limit (f_{max}), silicon amplifiers in D-band (110 - 170 GHz) employ multiple stages with relatively simple matching networks based on transmission line (TLINEs). To meet the wide band requirement, stagger-tuning of the networks is the simplest and most common approach [4][5][6]. Given the target bandwidth for the amplifier chain, closed-form design equations for the resonance frequency and bandwidth of the different networks are also available [7]. However, stagger-tuning penalizes the overall amplifier noise figure (NF) because the first stage provides gain only over a narrow bandwidth. The issue is even more relevant if the amplifier is designed to operate close to f_{max}, where the transistor gain drops and becomes comparable to its minimum noise figure (NF_{min}). In [7] and [8], staggering was arranged with the first stage centered at mid-band, thus sacrificing the NF at the extremes of the bandwidth. Similar issues also affect the amplifier linearity, making difficult to reach and maintain high compression performance over the full bandwidth. Optimal noise and linearity are achieved, in a multi-stage amplifier, when the gain is uniformly distributed among the stages and each stage displays a flat frequency response. This requires the use of multi-resonance broad-band matching networks, not yet widely explored in D-band amplifiers. At lower frequency, such kind of networks are widespread, being easily implemented with transformers [9] but, as frequency increases, the performance of integrated transformers degrades, and appropriate modeling becomes challenging. Starting from the operation of a dual-resonance doubly-tuned transformer, this paper elaborates an insightful design flow for wideband impedance scaling with TLINEs. The approach considers also practical constraints such as the need for DC decoupling, supply and bias of the different stages. The application to the design of a 3-stage D-band Low Noise Amplifier (LNA) is then proposed. Realized in a SiGe BiCMOS technology, the LNA achieves 28 dB gain with 127-168 GHz 3-dB bandwidth, NF down to 5.2dB and $>$ 2dBm output compression point with 30mA from 2V supply.

II. Broadband T-LINE-based Matching Networks

Broadband matching networks commonly implemented in RF and mmWave ICs leverage doubly-tuned transformers, allowing to simultaneously control the impedance transformation ratio and bandwidth through the turn-ratio and magnetic coupling. Nevertheless, in sub-THz bands, parasitic elements impair the performance of spiral inductors used in transformers, which exhibit low quality factor and low self-resonance frequency. In addition, the modeling of these structures is difficult, especially for single ended circuits, given that electromagnetic fields and current return paths are not constrained to a well confined area. On the other hand, transmission lines can be easily designed to overcome these issues, ensuring reliable modeling and enabling a modular and flexible approach.

This section proposes a step-by-step design flow for a broadband matching network that approximates the 4^{th} order response of a doubly-tuned transformer, but it is finally implemented with TLINEs, making it suitable for sub-THz silicon amplifiers.

A comprehensive analysis on 4^{th} order doubly-tuned transformer matching networks is available in [10]. Referring to Fig. 1 (a), when two LC tanks, characterized by natural

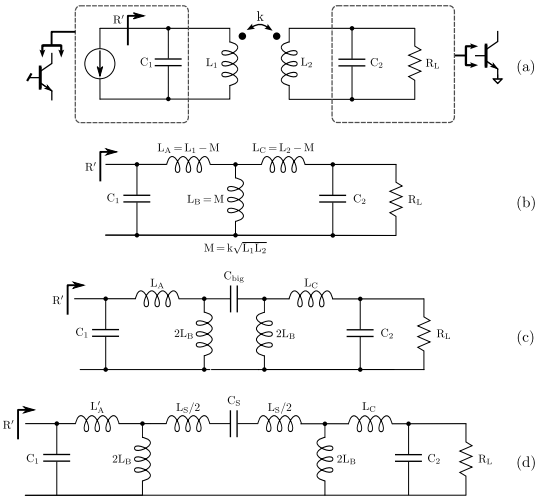

Fig. 1. Derivation of the matching-network circuit topology

frequencies ω_1 and ω_2, are magnetically coupled (with k the coupling factor), pole splitting occurs, and the overall network shows two resonances at ω_{L} and ω_{H}. In the simplified but common case of $\omega_1 = \omega_2 = \overline{\omega}$, the following relation holds:

$$\omega_{L,H} = \frac{\overline{\omega}}{\sqrt{1 \pm |k|}} \tag{1}$$

In [10], a compact set of equations is proposed to drive the network design (also in the general case of $\omega_1 \neq \omega_2$), such that the band-pass response can be easily controlled. Two key parameters that affect the frequency response are here recalled: the magnetic coupling factor k, which sets the bandwidth, and the loaded quality factor $\mathrm{Q_S}$, which describes how heavily the network is loaded by $\mathrm{R_L}$:

$$k = \frac{\omega_H^2 - \omega_L^2}{\omega_H^2 + \omega_L^2} \quad Q_S = \frac{R_L}{\sqrt{L_2/C_2}} \cdot \frac{1}{\sqrt{1-k^2}} \tag{2}$$

Finally, the product $k \cdot Q_S$ controls the in-band ripple and should be close to unity to reach a fairly flat in-band response. Still referring to Fig. 1 (a), the secondary tank, made of $\mathrm{C_2}$ and $\mathrm{R_L}$, absorbs the input impedance of the cascaded stage or, in the last stage, the impedance at the ground-signal-ground (GSG) pad. $\mathrm{C_1}$, instead, absorbs the capacitance at the output of the driving stage. Fig. 2 (red curve) plots the $\mathrm{S_{21}}$ of the transformer-based network in Fig. 1 (a) for a design example, of practical interest, which assumes that a load resistance $\mathrm{R_L} = 20\,\Omega$ is transformed into $\mathrm{R'} = 80\,\Omega$, seen at the primary side. The network components are listed in Table 1. The target now is to approximate the response of the network in Fig. 1 (a) with a feasible implementation based on TLINEs. First, Fig. 1 (b) presents an equivalent circuit obtained by replacing the transformer with its T-network equivalent circuit (considering the above design example, $\mathrm{L_A}$, $\mathrm{L_B}$, $\mathrm{L_C}$ are 23.7 pH, 4.3 pH and 2.6 pH, respectively). Interestingly, it is worth noticing that a realization of the network in Fig. 1 (b) offers higher flexibility in the impedance transformation ratio. In fact, when transformers are used, the impedance scaling is typically within $0.5 \sim 2$, limited by practical layout constraints on the turn ratio ($\mathrm{n} = \sqrt{\mathrm{L_2/L_1}}$ in Fig. 1 (a)). Instead,

Table 1. Values of the components employed in Fig. 1 (a)

$\mathrm{L_1}$ [pH]	$\mathrm{C_1}$ [fF]	$\mathrm{L_2}$ [pH]	$\mathrm{C_2}$ [fF]	k	$\mathrm{R_L}$ [Ω]
28	40	7	160	0.31	20

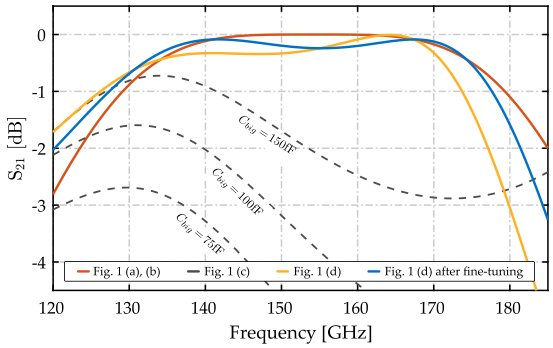

Fig. 2. Frequency responses of the different networks in Fig. 1

for the equivalent network of Fig. 1 (b) to be realizable, only the conditions $\mathrm{L_{A,C}} > 0$ must be verified. This implies $\mathrm{k^2} < \mathrm{R'/R_L} < 1/\mathrm{k^2}$ and, in the common cases of $\mathrm{k} \ll 1$, this greatly extends the available impedance transformation range. The network in Fig. 1 (b) does not provide DC-decoupling between the input and output ports. This is a fundamental feature of interstage matching networks, given the different supply and biasing requirements on the driver and the cascaded stage. To overcome this issue, $\mathrm{L_B}$ in Fig. 1 (b) may be split into a combination of two parallel inductors of value $2\mathrm{L_B}$, separated by a series capacitor, $\mathrm{C_{big}}$, as shown in Fig. 1 (c). $\mathrm{C_{big}}$ must behave as an AC short i.e. it has to be very large (ideally infinite). However, practical values are limited by parasitics, such as capacitance towards the substrate (ground), that make floating capacitors in excess of 100 fF unfeasible for applications above 100 GHz. The simulated $\mathrm{S_{21}}$ of the network in Fig. 1 (c), sweeping the values of $\mathrm{C_{big}}$ from 75 fF to 150 fF, is shown by the gray dashed curves in Fig. 2. The network response is remarkably distorted and a $\mathrm{C_{big}}$ much greater than 150 fF would be necessary to fit the ideal response.

Noticing that the role of $\mathrm{C_{big}}$ is to provide an AC-short between the two parallel branches of the network, it can be replaced with a series LC tank, as proposed in Fig. 1 (d). The series resonance frequency and quality factor (hence, the AC-short bandwidth) can be controlled by the values of $\mathrm{C_S}$ and $\mathrm{L_S}$. $\mathrm{C_S} = 70\,\mathrm{fF}$ and $\mathrm{L_S} = 13\,\mathrm{pH}$ are selected, such that the resonance frequency falls in-band. The resulting network response is plotted in Fig. 2 with the yellow curve. A deviation from the ideal (red) curve is observed as an unwanted loss toward the lower cut-off frequency (ω_{L}) and a sharper roll-off at high frequency (close to ω_{H}). This distortion is attributed to the extra poles added by $\mathrm{L_S - C_S}$ which increase the order of the network. The issue is easily solved with a fine (numerical) tuning of the other components. As an example, the blue curve, which approximates reasonably well the desired profile (with a deviation below 0.4dB), is achieved by adjusting $\mathrm{L_A}$ from 23.7 pH to 21 pH. All the inductors in the final network of Fig. 1 (d) are now easily implemented with short transmission-line stubs. Notice also that $\mathrm{L_S}$ is split into two parts (arbitrarily set equal in this example) such that each

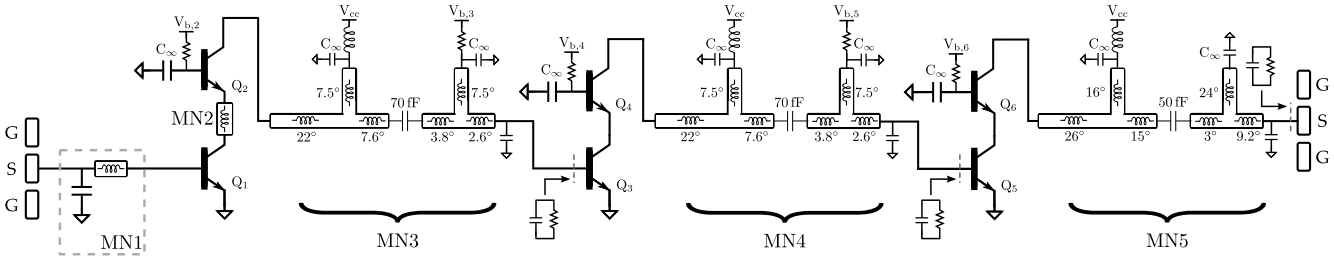

Fig. 3. Schematic of the 3-stage D-band amplifier

branch can absorb the equivalent inductance of the segments of a T-junction. Still, two portions of L_S absorb the stray inductance of the connections to C_S, which is realized as a multi-finger MOM capacitor. The final TLINE implementation of the matching network in the amplifier and the simulated performance with realistic (lossy) components are presented in the next section.

III. Amplifier Design

The proposed approach for wideband impedance matching is adopted to design a 3-stage D-band amplifier in a SiGe BiCMOS technology with the schematic shown in Fig. 3. The active stages are implemented with a cascode structure, giving a remarkably higher available gain than a single common-emitter or common-base transistor. All the multi-emitter HBTs have a drawn emitter area of $A_e = 2\,\text{x}\,5\,\text{x}\,0.2\,\mu\text{m}^2$. The devices are biased at a current density of $5\,\text{mA}/\mu\text{m}^2$, slightly below the peak point of f_{max} as a compromise between gain and noise performance. Looking at Fig. 3, the matching networks MN3, MN4, MN5 implement with TLINEs the lumped-element topology in Fig. 1 (d). The interstage networks MN3 and MN4 are identical while MN5, which interfaces the amplifier to the off-chip load, uses the same topology but with different components sizing. MN3 and MN4 provide a step-up of the impedance at the base of Q_3, Q_5. The latter is, in good approximation, a resistor $R_B = 14\,\Omega$ in series with a capacitor $C_{BE} = 120\text{fF}$. Given the low nodal quality factor ($Q = 1/(\omega R_B C_{BE}) \approx 0.63$ at 150 GHz), a RC parallel equivalent circuit with $R = 20\,\Omega$ well reproduces the impedance over a broad-band. The parallel RC model of the base impedance corresponds to R_L and a fraction of C_2 in the lumped-element schematic in Fig. 1 (d). An additional explicit

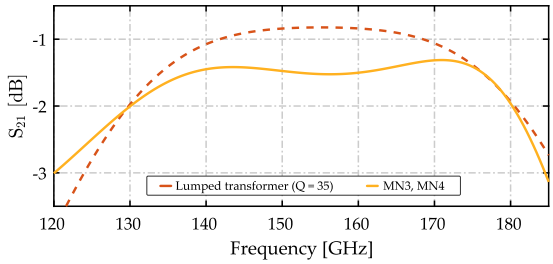

Fig. 4. S_{21} of MN3, MN4 (yellow line) and of the network of Fig. 1 (b) with lossy components (Q = 35 at 165 GHz).

MOM capacitor is added to reach the correct value of C_2. The capacitor C_1 in Fig. 1 (d) is fully implemented by the parasitic capacitance at the collector of the common-base HBTs Q_2, Q_4. TLINE stubs implement the network inductors. The TLINEs are realized as shielded microstrips with the signal trace in the topmost metal. From electromagnetic simulations, $Z_0 = 63\,\Omega$ and the quality factor is Q = 35 at 165 GHz. Once the desired values of the different inductors in the network of Fig. 1 (d) are found, the electrical length (θ_e) of the TLINE stubs are initially evaluated considering $L = Z_0 \tan(\theta_e)/\omega$ and then fine-tuned with simulations. Looking again at the schematic in Fig. 3, the grounded TLINE stubs are used to feed the supply to the driver stage and the bias voltage to the cascaded stage. The AC-short to ground is granted by capacitors labeled C_∞ (implemented as a stack of MIM and MOM caps). The simulated transmission performance (S_{21}) of MN3 and MN4 with real components is shown in Fig. 4 (solid line). When compared to the response of the network in Fig. 1 (b), assuming for the inductors the same Q = 35, it shows an additional $\approx 0.6\,\text{dB}$ transmission loss.
The first stage of the amplifier is optimized to improve the NF. MN1, in fact, transforms the $50\,\Omega$ off-chip impedance at the GSG pad into an impedance close to the one that minimizes the NF of the common-emitter transistor Q_1, while retaining a reasonable input match value ($S_{11} < -8\,\text{dB}$ in band). Due to the low gain available from the device, the noise contribution of the common-base Q_2 cannot be neglected. Matching network MN2 is included such that Q_2 is driven by its optimum noise impedance.

IV. Measurement

The amplifier is realized in ST Microelectronics' BiCMOS 55nm technology. The chip photograph is reported in Fig. 5, with an area of $730\,\text{x}\,258\,\mu\text{m}^2$, including GSG pads. Probing is performed with 75-μm pitch GSG Waveguide Infinity Probes connected to VDI WR6.5-VNAX network analyzer frequency extenders and an Agilent E8361C VNA. Small signal measurements (solid lines) are compared against post-layout simulations (dashed) in Fig. 6, showing 28 dB gain centered at 148GHz and a -3dB bandwidth that spans the 127∼168 GHz range. Noise figure, reported in green, is measured with a Keysight N8975A noise figure analyzer combined with a Farran WGNS-06 noise source and a Farran FBC-06 frequency block converter. The best noise figure achieved is 5.2 dB and it is maintained below 6.7 dB within the bandwidth. The amplifier shows unconditional stability, as expected. Power compression measurements are performed with ELVA-1 DPM-06 power meter, and the output 1-dB compression point is in excess of 2 dBm and fairly constant across the whole bandwidth, reaching a maximum value of

Table 2. Comparison with other SiGe Bipolar/BiCMOS amplifiers

	This work	[3]	[8]	[7]	[2]	[4]	[6]	[5]	[5]
Technology	55nm	130nm	130nm	55nm	130nm	55nm	90nm	120nm	120nm
f_t/f_{max}	320/370	250/370	300/500	320/370	300/500	320/370	300/500	200/265	200/265
# of stages	3	3	4	3	4	2	4	4	6
G_T [dB]	28	32.8	32.6	28.6	30	20.1	30	26	24
f_0 [GHz]	148	140	140	140	137.5	150	136	130	128
-3 dB BW [GHz]	41	23.2	52	64.3	55	24.5	28	13	20
GBW [GHz]	1030	1013	2218	1731	1739	248	885	259	317
P_{DC} [mW]	60	39.6	28	36	100	27	45	57	84
NF [dB]	5.2 - 6.6	7.8 - 9.5*	4.8 - 6.1	8.1*	7.5 - 8.2	-	6.2 - 8	-	-
P_{IP1dB} [dBm]	-25	-28.6	-37.6	-29.7*	-28	-	-	-	-
FoM_{ITRS}	**19.42**	16.88	7.14	5.05	4.3	-	-	-	-

* simulated value

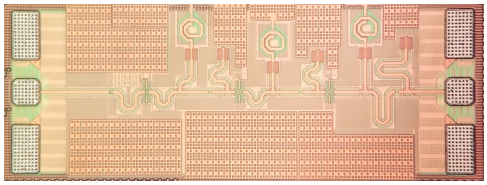

Fig. 5. Chip photograph

3.9 dBm at 135 GHz, with a power consumption of 60 mW. A comparison with the state of the art is reported in Table 2. The overall performance of the proposed amplifier is quantified with a figure of merit (FoM) introduced by ITRS and defined as[1]:

$$FoM_{ITRS} = \frac{G_T \cdot IIP_3 \cdot f_0}{(NF-1) \cdot P_{DC}} \tag{3}$$

The FoM allows to make a comparison with other amplifiers operating in D-Band and realized in similar technologies, for which all the necessary information is provided. As reported in the table, the FoM confirms the good performance of the proposed amplifier designed with broad-band interstage matching networks.

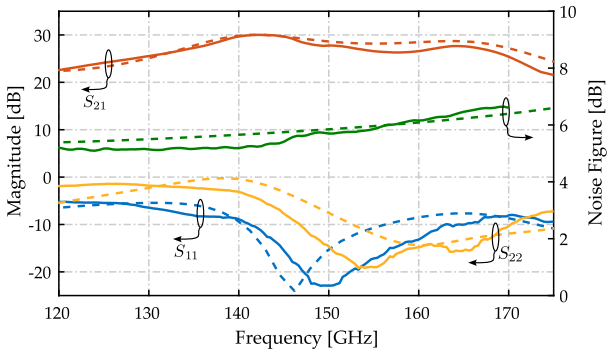

Fig. 6. Small-signal measurements

V. Conclusions

Broadband impedance matching has been discussed as a solution to improve the performance of D-band amplifiers over the widely used stagger-tuning technique. The fourth order frequency response of a doubly-tuned transformer is approximated with a matching network that can be easily implemented with TLINEs, more suited for designs operating in the sub-THz region. Design constraints such as DC decoupling are considered and intuitive considerations on the impact of different components on the frequency response are given. The concepts have been applied to the design of a broadband D-Band LNA. The measured performance, normalized with the amplifier FoM, compares favorably against other works operating in the same frequency range.

[1] IIP_3 estimated as P_{IP1dB} + 9.6 dB. Quantities are in linear scale.

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