Compact D-Band Passive Phase Shifters with Fine and Coarse Control Steps in BiCMOS-55nm

Lorenzo Piotto, Guglielmo De Filippi, Mahmoud M. Pirbazari, Andrea Mazzanti
Dept. of Electrical, Computer and Biomedical Engineering, University of Pavia, Italy

***Abstract*—Programmable phase shifters are key building blocks in emerging Sub-THz phased array transceivers. This work proposes different structures to implement compact passive phase shifters in D-Band (110 - 170 GHz). Tunable band-pass filters and variable-delay transmission lines are evaluated as phase shifters with fine control resolution over a limited range. To extend the range, 0°/180° and 0°/90° phase shifters are also investigated and implemented with a hybrid coupler and a switched λ/4 transmission line. Experimental results are presented on a test chip in a 9 metal BiCMOS technology with 55 nm MOS transistors used as switches. By combining the different structures, the full 0°/360° programmable range is covered from 120 GHz to 170 GHz with a size of only 0.13 mm^2. The estimated insertion loss is aligned with previous works, but the remarkable footprint reduction facilitates the adoption in dense sub-THz phase array systems.**

***Index Terms*—D-band, BiCMOS, phase shifter, phased-array**

I. Introduction

The demand for ultra-high-capacity wireless links in the network infrastructure of 5G and beyond is driving the development of integrated circuits above 100 GHz, where ultra-wide bands are available [1]. Within this scenario, D-Band (110 GHz – 170 GHz) is quickly gaining interest, and G-Band (140 GHz – 220 GHz) may follow. On the other hand, digital CMOS technologies keep getting closer to their intrinsic limitations (f_{max}) in these bands. Whilst more expensive semiconductors are available, they bring penalties in terms of cost, scalability and lack of integration of digital functions. SiGe BiCMOS fills the gap with f_t / f_{max} in the 350-500 GHz range and a roadmap to push the HBT frequency limits even further [2].

A key block in sub-THz applications is the phase shifter (PS), which enables active phased arrays for beam-forming and beam-steering, relaxing Power Amplifiers requirements and improving the SNR. Active PSs are based on the vector interpolation principle, typically characterized by high resolution but limited linearity, even at moderately high power consumption [3]. On the contrary, passive PSs offer excellent linearity at the expense of an increased area occupation and unavoidable insertion loss. To date, a very limited number of works explored programmable passive PSs in sub-THz bands [4]–[7], particularly in silicon. Switched transmission lines (TLINEs) were demonstrated in SiGe [5] and compound-semiconductor technologies [6], but they require a large area that does not fit a sub-THz phased-array system, with antenna spacing of 1 mm or less. A PS which combines reflective-type hybrid couplers and an active stage for phase inversion was proposed at 120 GHz in SiGe BiCMOS, proving low insertion loss with fine phase control resolution but over a narrow bandwidth [4].

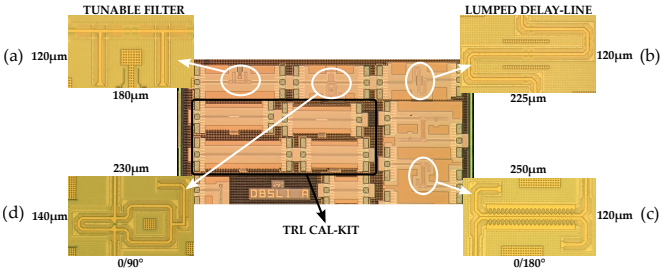

Fig. 1. Chip photo of the realized passive phase shifters.

This work investigates passive D-band PSs leveraging the availability of good MOS switches and a 9-level metal stack, with two thick top layers, in the SiGe BiCMOS-55nm of STMicroelectronics. Fig. 1 shows the photograph of the realized test chip, which includes also a TRL cal-kit used to de-embed pads and access lines from measurements. The PSs are classified into fine (1) and coarse (2) phase-control steps. The former feature a digitally-controlled phase shift in small steps but, to limit the insertion loss, the maximum range is limited. The latter provide a 1-bit phase control (nominally 0°/90° and 0°/180°). By cascading fine- and coarse-control PSs, the full 0°/360° can be covered with fine control resolution and limited insertion loss. Design and measurements of the PSs are presented in Sec. II and Sec. III, followed by a discussion and conclusion in Sec. IV.

II. Phase Shifters with Fine Control Steps

Two different approaches are investigated for PSs with a fine control step. The first is based on 4th order band-pass filters with tunable center frequency. Such kind of response may be achieved through magnetically coupled resonators, shown in Fig. 2a. An analysis of these networks is presented in [8]. If the components (R, L, C, k) are sized such that the two pairs of complex conjugate poles provide a flat in-band response, the phase of the transfer function is fairly linear across frequency, with a variation of π radians within the -3 dB bandwidth, $\mathrm{BW}_{-3\mathrm{dB}} = f_H - f_L$. Therefore, $\mathrm{d}\phi/\mathrm{df} \approx \pi/\mathrm{BW}_{-3\mathrm{dB}}$. If the filter center frequency, f_0, is shifted by Δf_0 by varying the net-

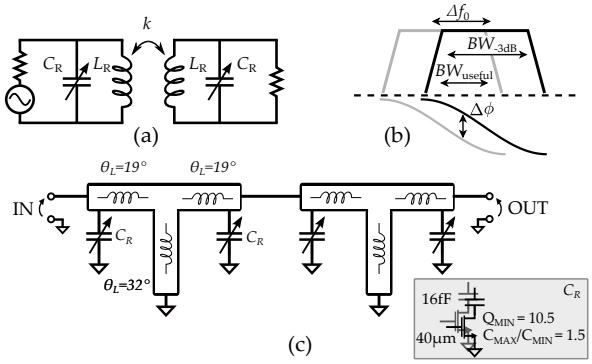

Fig. 2. Coupled-resonator band-pass filter (a) and transfer function (amplitude/phase) variation by tuning the center frequency (b). Schematic of the implemented network (c).

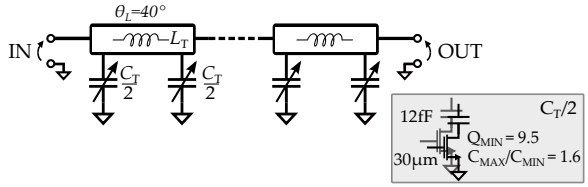

Fig. 3. Fine-resolution phase shifter realized as a transmission line periodically loaded by digitally-tuned capacitors.

work capacitors (gray plot in Fig. 2b), the signal experiences a phase shift variation:

$$\Delta\phi \approx \frac{\pi}{BW_{-3dB}} \cdot \Delta f_0 \tag{1}$$

However, to avoid attenuation when the network transfer function is translated, the useful bandwidth ($\mathrm{BW_{useful}}$) is lower than $\mathrm{BW_{-3dB}}$. Looking at Fig. 2b, $\mathrm{BW_{useful}} = \mathrm{BW_{-3dB}} - \Delta f_0$ and making use of (1):

$$\mathrm{BW_{useful}} = \mathrm{BW_{-3dB}} \left(1 - \frac{\Delta\phi}{\pi}\right) \tag{2}$$

From (2), given a target $\mathrm{BW_{useful}}$, the wider is the desired maximum phase variation, the larger must be $\mathrm{BW_{-3dB}}$. On the other hand, $\mathrm{BW_{-3dB}} \propto 1/(\mathrm{RC})$, thus an upper bound on $\mathrm{BW_{-3dB}}$ (and hence $\Delta\phi$) is finally set by the minimum variable capacitors that can be reliably implemented to achieve the required tunability of f_0. To extend the attainable phase shift, multiple replicas of the networks can be cascaded. Two identical band-pass cells are used in the implemented PS, giving twice the phase shift range with a marginal bandwidth reduction. The schematic is shown in Fig. 2c. The coupled inductors of Fig. 2a are replaced by their equivalent T-network, implemented with short TLINEs that provide lower loss compared to magnetically-coupled circular coils. The TLINEs are shielded microstrips with the signal routed in the topmost metal layer and display a quality factor Q = 35 at 165 GHz. The network center frequency is digitally tuned by a bank of four switched MOM capacitors. The switches are nMOS with W/L = 40 um / 55 nm, implemented in triple well to limit the bulk parasitic capacitance. Each MOM-switch combination features $\mathrm{C_{MAX}}$=16 fF with $\mathrm{C_{MAX}/C_{MIN}} = 1.5$ and minimum

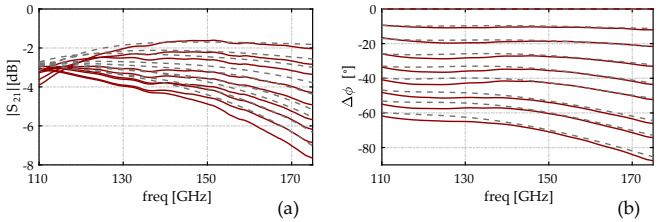

Fig. 4. Measurements (solid-red) and simulations (dashed-gray) of forward gain (a) and phase response (b) of the tunable band-pass filter.

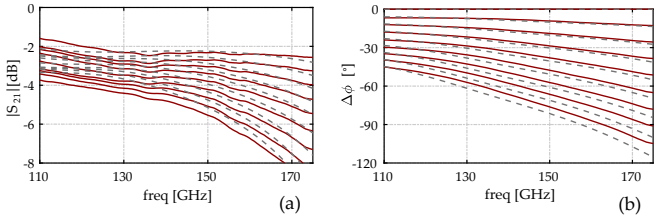

Fig. 5. Measurements (solid-red) and simulations (dashed-gray) of forward gain (a) and phase response (b) of the tunable-delay line.

quality factor $\mathrm{Q_{MIN}} = 10.5$. The band-pass cells are sized for a center frequency of 150 GHz and 90 % fractional bandwidth. The capacitors bank shifts the center frequency by ±10 % thus, using (2), each cell introduces roughly 35° of programmable phase shift while the cascade of the two cells provides 70°.

The alternative fine-step PS investigated consists of a transmission line with tunable propagation delay. The schematic is shown in Fig. 3. Short sections of TLINEs, which approximate inductors of value $\mathrm{L_T}$, are interleaved with digitally switched capacitors $\mathrm{C_T}$. The overall network, composed of N sections, behaves as a low pass filter. The cut off frequency, defined as the frequency where the input impedance becomes purely reactive (i.e. no active power can be injected into the line) is $\omega_T = 2/\sqrt{L_T C_T}$. For a signal at angular frequency ω_0 sufficiently lower than ω_T, the network well approximates a TLINE with Z_0 and group delay τ_D given by:

$$Z_0 = \sqrt{\frac{L_T}{C_T}} \qquad \tau_D = N \cdot \sqrt{L_T C_T} \tag{3}$$

The group delay, and hence the network phase shift ϕ, are tuned by capacitors $\mathrm{C_T}$. If each capacitor is switched between $\mathrm{C_{T,MIN}}$ and $\mathrm{C_{T,MAX}}$, the variation of τ_D and of the network phase shift (in radians) are:

$$\Delta\tau_D = N\sqrt{L_T C_{T,MIN}} \left(\sqrt{\frac{C_{T,MAX}}{C_{T,MIN}}} - 1\right) \quad \Delta\phi = \omega_0 \Delta\tau_D \tag{4}$$

The variable capacitors $\mathrm{C_T}$ are realized with a bank of four digitally switched MOM capacitors of 12.5 fF, giving $\mathrm{C_{T,MAX}} = 50$ fF. The nMOS are sized with W / L = 30 um / 55 nm, leading to $\mathrm{C_{T,MAX}/C_{T,MIN}} = 1.6$ and $\mathrm{Q_{MIN}} = 9.5$. The length of each piece of TLINE between consecutive capacitors is set to approximate $\mathrm{L_T} = 50$ pH such that ω_T is greater than 2π 200 GHz. From (4), the delay variation of one cell (N=1) is $\Delta\tau = 0.34$ ps, corresponding to a phase shift of 17.5° at 150 GHz. To reach a total phase shift variation comparable with the tunable band-pass filter, the structure is implemented with four (N = 4) cascaded $\mathrm{C_T}$/2-$\mathrm{L_T}$-$\mathrm{C_T}$/2 cells .

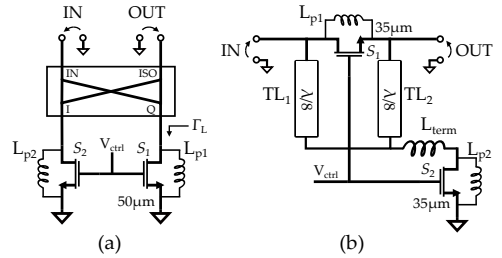

Fig. 6. Coarse-resolution phase shifters to realize 180° (a) and 90° (b) phase steps.

The chip photos of the fine-control PSs are shown in Fig. 1a and Fig. 1b with core size of $180\,\mathrm{x}\,120\,\mu\mathrm{m}^2$ and $225\,\mathrm{x}\,120\,\mu\mathrm{m}^2$, respectively. The measured forward gain and phase of the tunable band-pass filters are plotted in Fig. 4 as solid lines and compared with simulation (dashed). The programmable phase shifting range is $>60°$ at 110 GHz and 85° at 170 GHz with phase steps between 10° and 13°. The insertion loss is <4 dB at the minimum phase shift and rises to 7 dB at 170 GHz for the maximum phase shift. The insertion loss normalized to the achievable phase shift is 65 mdB/° at 110 GHz and 80 mdB/° at 170 GHz. Fig. 5 reports the results for the variable-delay TLINE. The phase plot in Fig. 5b shows an almost linear phase shift over frequency, as a result of the constant group delay rather than constant phase shift. The insertion loss is around 2 dB at the minimum phase shift and rises to 4 dB at 110 GHz and 8.3 dB at 170 GHz at the maximum phase shift of 100°. The normalized insertion loss is 77 mdB/° at 110 GHz, and 83 mdB/° at 170 GHz, comparable to what measured on the the tunable filter. The return loss, not shown, is <10 dB at all the phase settings for both the tunable filter and delay line.

III. Phase Shifters with Coarse Control Steps

The physical size and insertion loss of the structures presented in the previous Section increase proportionally to the desired range of programmable phase shift. Thus, to cover a wider range while maintaining a fine control resolution, it is more convenient to cascade those structures with networks that provide a large phase shift in a single coarse step, limiting the insertion loss and silicon area. A 0°/180° and a 0°/90° PSs are proposed in this section.

In [6], 0°/180° are achieved by using two hybrid couplers and two SPDT switches in a compound semiconductor technology. The structure proves low insertion loss (also thanks to the excellent performance of HEMTs) and a flat phase across frequency, but requires large chip size. On the other hand, while being desirable, a flat phase response is not mandatory if the block is to be cascaded with fine-control PSs, because its phase error versus frequency can be corrected by the latter. The implemented 0°/180° PS, shown in Fig. 6a, uses only one hybrid coupler and two grounded switches, leading to a very compact size. The circuit works as a reflective-type PS. The input signal, $\mathrm{S_{IN}}$, is equally split at the I/Q ports of the coupler. If an identical impedance, $\mathrm{Z_L}$, with non-zero reflection coefficient (Γ_L) loads the I/Q ports, the reflected signals sum

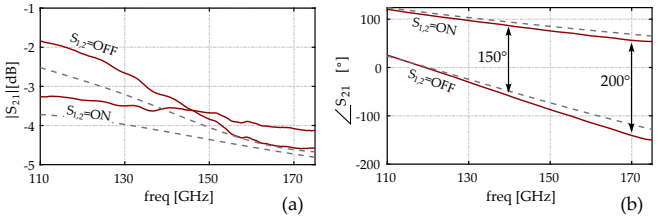

Fig. 7. 0/180° forward gain (a) and relative phase shift (b) compared against simulation (dashed-gray).

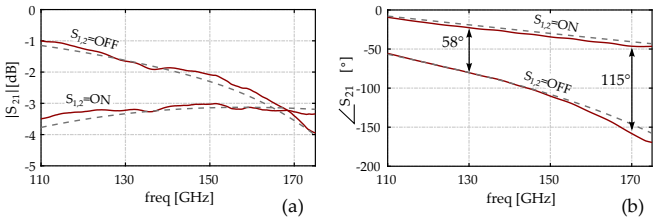

Fig. 8. 0/90° forward gain (a) and relative phase shift (b) compared against simulation (dashed-gray)

up at the ISO port, giving the output signal $\mathrm{S_{OUT}}$. Neglecting losses, the following relation holds:

$$\left|\frac{S_{OUT}}{S_{IN}}\right| = |\Gamma_L|^2 \qquad \angle\frac{S_{OUT}}{S_{IN}} = -90° + \angle\Gamma_L \tag{5}$$

The I/Q ports are terminated by the switches $\mathrm{S_{1,2}}$, implemented with nMOS transistors, yielding ideally $\Gamma_\mathrm{L} = \pm 1$ in the OFF and ON state, respectively. Using (5), $\mathrm{S_{IN}}$ is transferred to the ISO port with the same magnitude but ±90° phase, corresponding to a 180° relative phase variation. The finite channel resistance and the parasitic capacitance of the nMOS switches introduce signal loss and deviation from the ideal 180° phase. The transistors are sized with $\mathrm{W/L} = 50\,\mu\mathrm{m}\,/\,55$ nm to achieve $\mathrm{r_{on}} = 7\,\Omega$, while the OFF-state parasitic capacitance is resonated out by the parallel inductors $\mathrm{L_{p1,2}} = 40$ pH, implemented with bent TLINEs stubs visible on the chip layout in Fig. 1c. The hybrid coupler is realized with 230 μm-long coupled lines. The core size of the 0°/180° PS is $250\,\mu\mathrm{m}\,\mathrm{x}\,120\,\mu\mathrm{m}$.

A 0°/90° phase shifter can be implemented by selecting the I or Q output of a 90° hybrid coupler, but with an intrinsic insertion loss of 3dB [6]. To avoid this loss, the proposed 0°/90° PS leverages a λ/4-long TLINE with a bypass switch. The schematic is drawn in Fig. 6b. Inductors $\mathrm{L_{p1,2}} = 60$ pH, in parallel to the nMOS switches $\mathrm{S_{1,2}}$, resonate with transistors parasitic capacitances to rise the impedance and improve isolation when $\mathrm{S_{1,2}}$ are OFF. In this condition, $\mathrm{L_{term}}$ is floating and the signal flows through $\mathrm{TL_1}$ and $\mathrm{TL_2}$, experiencing the 90° phase shift of the λ/4 total length. When $\mathrm{S_{1,2}}$ are ON, $\mathrm{S_1}$ shorts the input to the output, thus the phase shift is ideally 0°. In this situation, $\mathrm{TL_1}$ and $\mathrm{TL_2}$ are shunted and the top port is connected to the input/output. Not to compromise the insertion loss and reflection coefficient, the bottom port of $\mathrm{TL_{1,2}}$ is terminated by $\mathrm{L_{term}} = 25$ pH (grounded on one side by $\mathrm{S_2}$). In fact, $\mathrm{TL_1}$ and $\mathrm{TL_2}$ behave like a single λ/8 TLINE with half the characteristic impedance, $\mathrm{Z_0}/2$. $\mathrm{L_{term}}$ is thus sized for an impedance of $+\mathrm{jZ_0}/2$, such that a high impedance

TABLE I
MEASUREMENTS SUMMARY AND COMPARISON

	[4]	[5]	[6]			This work			
						Tunable Filter	Tunable TLINE	0°/90°	0°/180°
Technology	120 nm SiGe	130 nm SiGe	GaAs			55 nm SiGe			
Frequency [GHz]	116 - 128	110 - 170	110 - 170			110 - 170	110 - 170	130 - 170	140 - 170
Phase control range [°]	360	260 @110 GHz 405 @170 GHz	180±2	87±2	47±4	62 @110 GHz 84 @170 GHz	47 @110 GHz 100 @170 GHz	58 @130 GHz 115 @170 GHz	145 @140 GHz 200 @170 GHz
Max Insertion Loss [dB]	8*	24 @110 GHz 23 @170 GHz	5 @110 GHz 6.5 @170 GHz	6	6.5	4 @110 GHz 7 @170 GHz	4 @110 GHz 8.3 @170 GHz	3.2	3.5 @140 GHz 4.5 @170 GHz
Phase Resolution [°]	11.25	17 @110 GHz 27 @170 GHz	-	-	-	7 @110 GHz 13 @170 GHz	7 @110 GHz 13 @170 GHz	-	-
Area [mm^2]	0.19	1.17	0.94	0.56	1.25	0.022	0.027	0.032	0.030
Normalized Insertion Loss † [mdB/°]	-	92 @110 GHz 57 @170 GHz	28 @110 GHz 36 @170 GHz	69	15	65 @110 GHz 83 @170 GHz	77 @110 GHz 83 @170 GHz	60 @130 GHz 28 @170 GHz	24

* Including buffer/s † $\mathrm{InsertionLoss}/\Delta\phi$

(ideally open circuit) is seen at the top port of TL_1,TL_2. The size of the nMOS switches is set to W/L=35μm / 55nm as a compromise between insertion loss and phase error, caused by channel resistance and device capacitances, respectively. Inductors $\mathrm{L}_{\mathrm{p1,2}}$ and $\mathrm{L}_{\mathrm{term}}$, visible on the chip photo in Fig. 1, are realized with TLINEs. The core size of the 0°/90° phase shifter is 230 μm x 140 μm.

The simulated and measured magnitude and phase response of the 0°/180° and 0°/90° PSs are plotted in Fig. 7 and Fig. 8, respectively. The 0°/180° PS provides the 180° phase inversion at 160 GHz. The phase error from 180° is within 30° from 140 GHz to above 170 GHz. The insertion loss in this band is below 4.5 dB, which corresponds to < 24 mdB/°, remarkably lower than what achieved by the fine-control PSs. The 0°/90° PS introduces the 90° relative phase difference at 160 GHz with a deviation lower than 30° from 130 GHz to above 170 GHz. The insertion loss is within 2 - 4 dB which corresponds < 60 mdB/°. The return loss for the two PSs, not shown, is below -10 dB.

IV. Discussion and Conclusions

The measured results presented in the previous Sections are summarized in Table I and compared with the few other integrated PSs operating in D-band. The insertion loss of the proposed PSs is aligned with previous works, with area occupation which is significantly reduced, simplifying the adoption in dense Sub-THz phased array systems. Moreover, the implemented structures offer high flexibility by providing different phase shift control range and resolution. By cascading fine- and coarse-step PSs, a large programmable phase shift range can be covered maintaining the fine resolution in the phase control. As an example, Fig. 9 shows all the possible magnitude and phase responses achieved by cascading the measured S-parameters of 3 tunable band-pass filters with the 0°/90° and the 0°/180° PSs. Looking at Fig. 9b, the chain covers more than 360° with a fine resolution from 120 GHz to 175 GHz. The corresponding insertion loss for a relative phase shift programmed from 0° to 360°, marked with red dots in Fig. 9, is between 12 dB and 16 dB at 120 GHz and between 14 dB and 20 dB at 175 GHz. The maximum loss, normalized to the 360°, is below 55 mdB/°, still comparable or better than the other PSs in Table I. The footprint of the five cascaded block is extremely small. The estimated silicon area, of only 0.13 mm^2, remains remarkably lower than the area occupation of previously reported PSs in D-band.

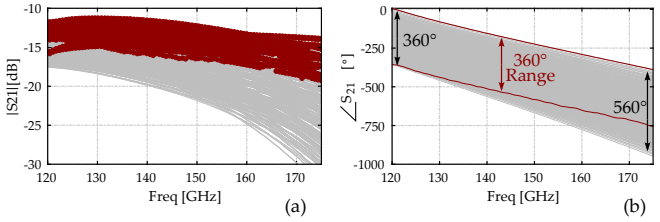

Fig. 9. S_{21} amplitude (a) and phase (b) response of the cascaded fine and coarse phase shifters

V. Acknowledgments

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