Embedded component packaging for D-band radio systems

Mario Schober
AT&S
Leoben, Austria
m.schober@ats.net

David del Rio
Ceit & Tecnun, University of Navarra
Donostia, Spain
ddelrio@ceit.es

Alberto Chico
CELESTIA TTI
Santander, Cantabria, Spain
achico@ttinorte.es

Vladimir Ermolov
VTT Technical Research Center of Finland
Espoo, Finland
vladimir.ermolov@vtt.fi

***Abstract*— The paper presents an embedded component packaging platform for D-band radio systems. The embedded component packaging is highly reliable due to optimal protection of the embedded components and good heat dissipation. Key elements of the platform are tested. The testing shows promising results in terms of insertion loss, achieving~0.5 dB per transition at 150 GHz. However, isolation of the RF lines feeding phased array chips should be improved in the next version of the platform.**

Keywords— packaging, millimetre-wave, D band, phased array

I. Introduction

Data traffic in future 5G and beyond 5G mobile networks requires the usage of large bandwidths, which are available only in the high millimetre-wave and sub-terahertz regions [1-2]. Free spectrum in D-band (130 to 175 GHz) offering a vast bandwidth is considered as a strong candidate for high capacity backhaul networks for 5G and beyond [3]. Successful commercialization of D-band radio systems is not possible without advanced integration technologies providing size miniaturization, cost reduction and performance enhancement of the systems. Several packaging technologies have been demonstrated for D-band applications: low temperature co-fired ceramic (LTCC) [4], integrated passive device (IPD) [5] and thin-film processing on alumina substrate [6]. LTCC provides multilayer metal structures, but it is not a cost-effective solution in large scales. IPD technology enables conductive layers inside polymer films on top of a carrier substrate, but the layer thickness and the number of layers is usually limited. Thin-film processes usually have only a single patterned layer over a ground plane layer. Such process is not feasible for complex integrated systems like phased antenna arrays, where several layers are required to route the DC, control and high frequency RF lines.

A cost-effective and low-loss multilayer integration technology utilizing PCB processing techniques was demonstrated for D-band applications [7,8]. The technology was based on integration of an antenna array in an advanced PCB substrate and flip chip bonding of the MMIC on the substrate. Required line widths and gaps down to 50 um were reached by using SAP (semi-additive processing) on outer copper layers. HDI-any layer (high density interconnect) construction technology was used to have multiple layers. HDI-any layer technology allowed to have minimum size (down to 80 um) laser vias between PCB metal layers. Multi-layer organic materials were used as the substrate. The technology demonstrated good performance in D band, but 4 layers of metal in the platform are not enough for realizing all needed routing of RF, DC and control signals in a transceiver with a big antenna array requested by practical applications. Additionally, thermal management of the system was a problem, preventing the scalability of the system. To resolve those faced challenges, an embedded-component packaging platform for D-band radio systems was proposed within the framework of the EU H2020 project DRAGON. Such packaging allows embedding of MMIC chips and passive components into the printed circuit board, facilitating the interconnections and thermal dissipation.

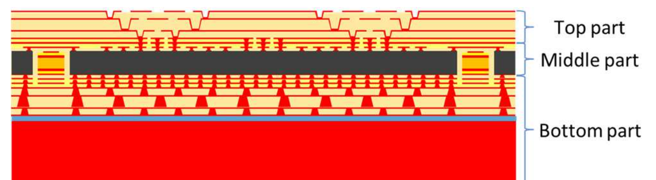


Fig. 1. Cross-section view of the integration platform stack-up.

A cross-section view of the platform stack-up is shown in Fig. 1. The system includes 16 metal layers and MMIC chips and capacitors are embedded in the PCB substrate (black square in Fig. 1). The platform consists of three parts. A top part (5 metal layers) is used for antenna implementation. A middle part (6 metal layers) is used for MMIC and capacitors embedding, RF routing, DC planes and control signals. A bottom part (5 metal layers) and a copper layer sintered to the backside of the

PCB are used for a heat management of the system. This extends the effective heat dissipation area as much as possible before a TIM interface to a heatsink.

The embedded component packaging is highly reliable due to optimal protection of the embedded components and good heat dissipation. It increases the possible density of active and passive components. Miniaturization of the system allows keeping signal short and losses to a minimum.

The performance of the top antenna level of the platform was successfully demonstrated in [9]. In this paper, we present preliminary testing results of a part of the platform, including the embedding of the MMIC and RF interconnections.

II. FABRICATION

The operation of the integration platform was verified with a 4-channel SiGe transmitter MMIC designed for a D band active antenna array. The MMIC consists of a VGA, a four-way splitter and four identical chains made of a driver, a phase shifter, and a PA. Details of the MMIC and its performance are presented in [8]. In this work, the pads of the transmitter chip are adapted for compatibility with the proposed integration platform. In addition, a test chip with a 500-µm side-shielded microstrip transmission line was fabricated in the same technology (STMicroelectronics' 55-nm SiGe BiCMOS) for standalone study of D-Band interconnections in the proposed platform.

Copper pillars (Cu-pillars) were fabricated on the chip for interconnections of the chip and PCB metal layers. The pillars have a diameter of 30 µm and a height of 25µm. Cu-pillar dimensions are selected to provide optimum RF performance of the interconnection. The height of the pillars is processed with an accuracy of +/- 2µm. The pillars were fabricated on top of copper pads with 50µm diameter and 5µm height and placed on Al-pads of the chip. Copper pads and pillars were fabricated on a wafer before wafer dicing. The view of the pillar is shown in Fig. 2.

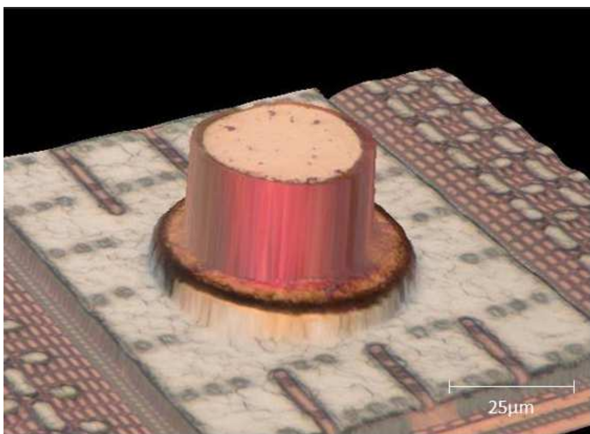


Fig. 2. A copper pillar on a top of MMIC chip.

The cavities for the MMIC chip and bypass capacitors needed for the DC feeds of the MMIC were fabricated into the center core of the PCB. The chip and capacitors were placed in the cavities (see Fig. 3). They are surrounded with resin material, and completely encapsulated in the PCB.

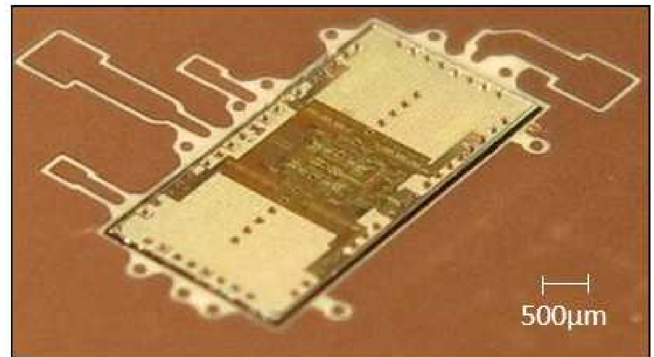


Fig. 3. MMIC chip embedded in the centre core of the PCB.

Ajinomoto Buildup Film (ABF) resin material (ε_r=3.5 and tanδ=0.0033) is laminated above the chip and capacitors. The Cu-pillars on top of the chips permeate the resin completely and have the same height as the thickness of the laminated resin. Thus, the Cu-pillars create interconnections from chip to the PCB layers above the chip with the high position accuracy without any risk of harming the chip by the thermal impact of a laser drilling process to the chip. A laser drilling process is used for connection of more robust integrated capacitors. For such kind of chip embedding technology, a copper free base material like ABF is essential and is not possible with common Resin Coated Copper (RCC) material. The image of the chip covered by a layer of ABF is shown in Fig. 4.

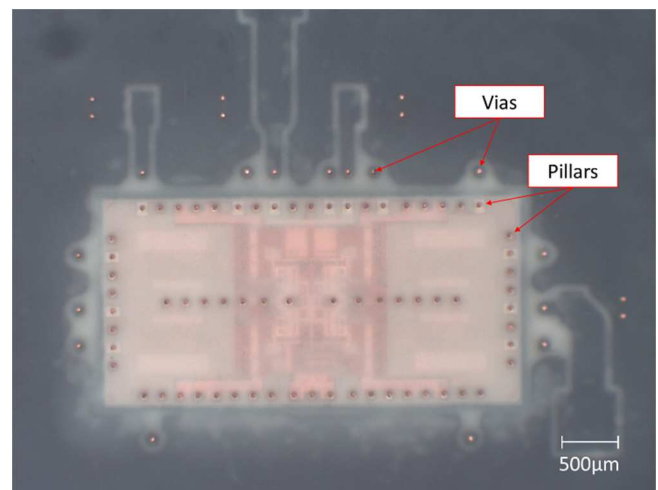


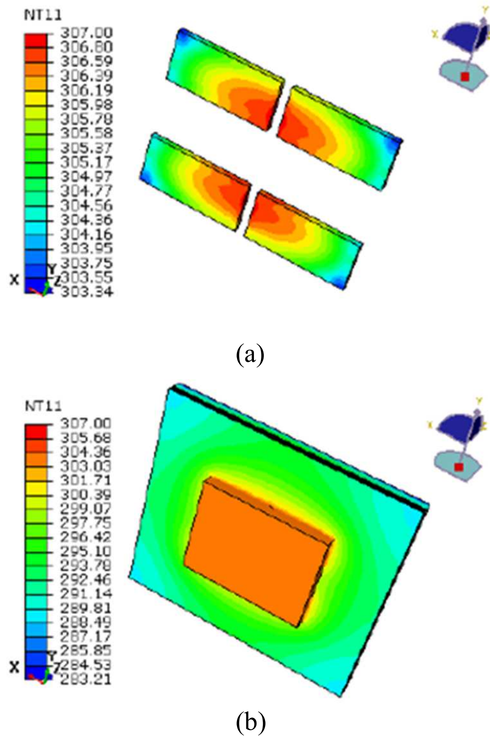
Fig. 4. MMIC chip embedded in the centre core of the PCB and covered with resin. Pillars reaching through the resin can be seen. Laser drilled micro vias are visible around the chip.

Copper is sputtered on top of the resin material with a Physical Vapor Deposition (PVD) process. Then Semi Additive

Technology (SAT) is used for fabrication of interconnection structures with high accuracy.

After integration of the active and passive devices using ABF, the remaining buildup layers were done with MEGTRON 7 Resin Coated Copper (RCC) material (ε_r=2.63 and tan δ=0.0031) from Panasonic. The simulated propagation loss of a 50-Ω transmission line in this material is 2.6 dB/cm. Same as ABF, MEGTRON 7 (RCC) has no glass inside because of its very low thickness. Metal layer-interconnection is done by UV / CO_2 laser drilling process with a local alignment on the array level to gain the highest layer to layer alignments. Vias are plated with Cu during followed SAT lithography process. The whole PCB buildup of the test structure has 10- metal layers separated by the core made of a 100µm thin MEGTRON 7 R-5785(N) laminate and 3313 glass-type.

Different types of thermal vias configurations were studied for optimization of the heat transfer from MMIC chips to the heat spreader. The thermal vias shown in Fig. 6a were selected due to a good compromise between efficiency of heat transfer and complexity of the fabrication. The temperature difference between MMIC chip and a bottom of the heat spreader is 3° C only. Fig. 5a shows temperature distribution on MMIC chips for a case of 4 chips. Fig. 5b presents a temperature distribution on the bottom of the heat spreader. Thus, utilization of the heat spreader provides the homogeneous distribution of heat in the substrate.



(a)

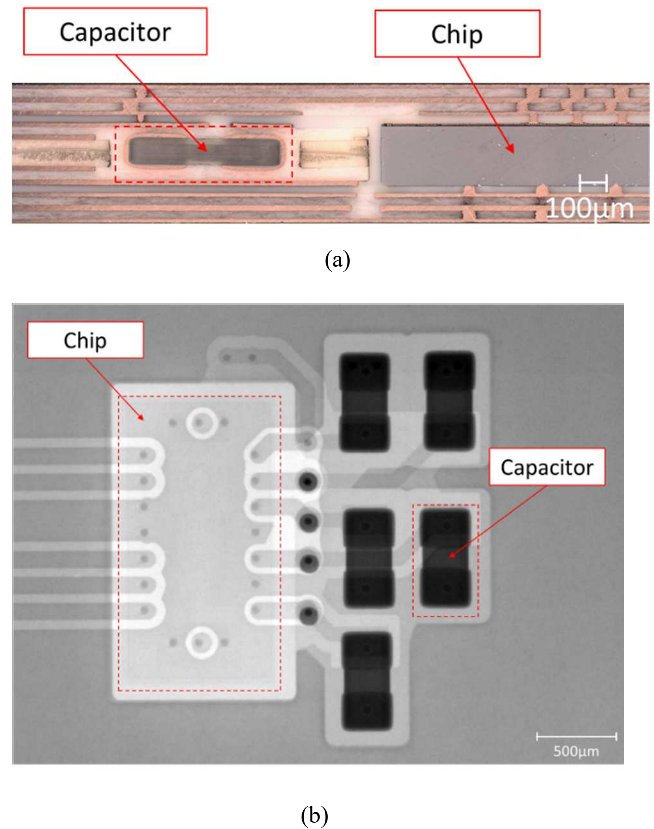
(b)

Fig. 5 Temperature distribution of on MMIC chips (a) and on the bottom of the heat spreader.

The using of glass-free material leads to a high risk of non-linear panel deformation in X- and Y-direction. Therefore, a local card level flexible alignment system was used for compensation of position deviations. It allows to achieve a sufficient layer to layer accuracy and stay within the specified 40-µm annular ring of Cu-pads.

Direct Immersion Gold (DIG) was deposited on the top surface of the chip test board. This special kind of surface finishing is free of nickel, and it is ideal for high frequency applications.

A cross section and x-ray image of the fabricated test structure are shown in Fig. 6.



(a)

(b)

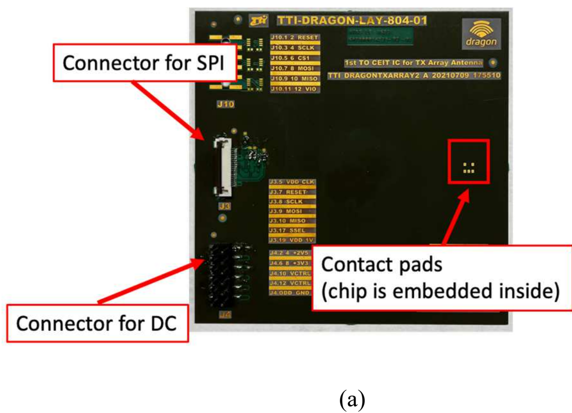
Fig. 6. Cross section (a) and X ray image(b) of the fabricated test structure.

The top view of the test PCBs constructed with the chips inside is shown in Fig. 7. Two different PCBs are fabricated. The PCB for the transmitter phased array also includes connectors for the SPI and DC signals (Fig. 6a). The chip with transmission lines is embedded in a second test PCB, shown in Fig. 6b. In both cases, pads with a 150-µm pitch are placed on the PCB top layer, internally connected to the RF signals of the chips, so that on-wafer probes can be used for characterization of the embedded chips.

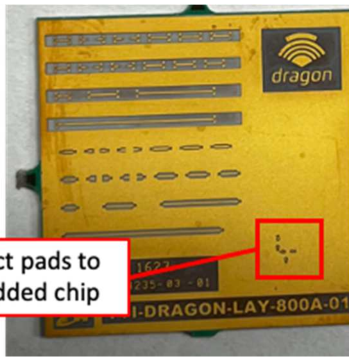
III. Results and Discussion

The S-parameters of the test structures were measured at D-band (110–170 GHz) using PNA-X N5245A with WR6.5-VNAX extenders and ground-signal-ground (GSG) probes with

150-µm pitch. The line-reflect-reflect-match (LRRM) calibration method is used in the measurements, thus the effects of the GSG probes are de-embedded from the presented results and the measurement reference plane is placed at pads on the PCB top layer.



(a)

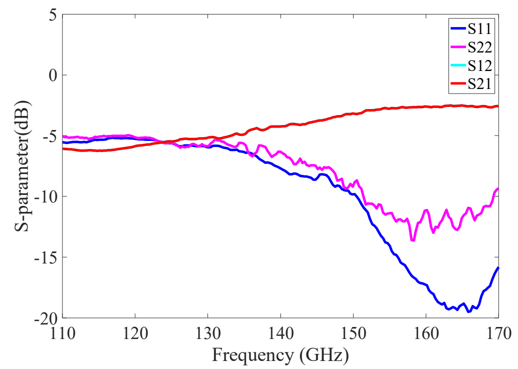


(b)

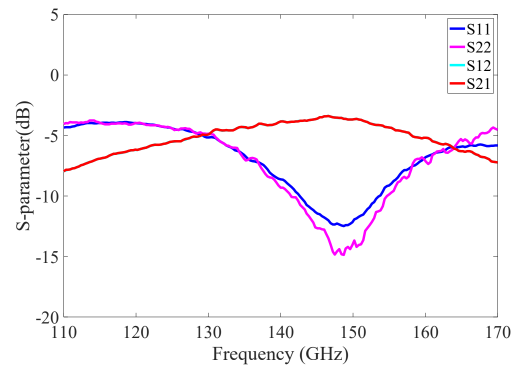
Fig. 7. PCBs for testing the integration platform: (a) 4-channel phased array TX (b) Test chip with transmission lines.

As mentioned above, to evaluate the performance of the transitions from PCB to the embedded chip in the proposed platform at D-Band frequencies, a test chip with transmission lines is embedded in a separate PCB. The S-parameters of the on-chip 500-µm microstrip transmission line measured on a bare die and presented in Fig. 8a. The insertion loss is around 2.5 dB, including the chip pads. Then, the PCB which includes a chip with the same transmission line embedded inside is measured. The S-parameters measured are shown in Fig. 8b. In this case, the measured insertion loss is 3.4 dB, which accounts for the transmission line itself (2.5 dB), two Cu-pillars and two PCB vias. Therefore, it can be concluded that each PCB-to-embedded-chip transition introduces an insertion loss below 0.5 dB, which is very good at these frequencies.

It can be observed in Fig. 8b that the embedded MMIC exhibits the best impedance matching (S11 and S22 < -10 dB) around 150 GHz. This was expected, since all the transitions were optimized for this frequency. These results validate the integration approach for these frequencies, as well as the employed design and simulation procedures.



(a)



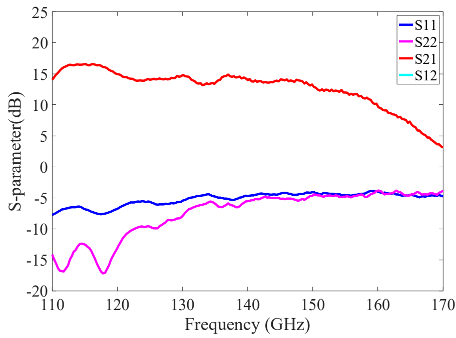
(b)

Fig. 8. Measured S parameters of a 500-um transmission line (a) on a bare MMIC chip and (b) after embedding the MMIC chip into the PCB.

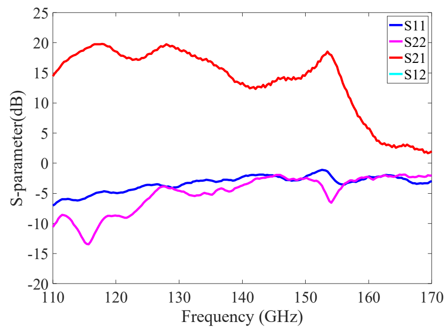
Once the transition is validated, measurements were conducted over the 4-channel D-band phased array transmitter. Fig. 9 shows the test results of a channel in the 4-channel transmitter MMIC for both the bare chip (Fig. 9a) and the chip embedded in the PCB (Fig. 9b). No significant degradation in the gain is observed, which proves the suitability of the assembly technology. The impedance matching is poor in both cases, mainly because the circuits inside the chip were not optimized for the new pad dimensions. Ripples in the S11 and S22 are the main cause for the observed gain ripple.

Fig. 10 shows the measured S-parameters for all four channels of the embedded MMIC. It can be observed that strong ripples are presented in channels 4 and 1, the closest to the RF input, while channels 2 and 3 have a flatter frequency response. The reason is a non-negligible output-to-input coupling of the signals, due to the long pillars and vias. According to EM simulations in HFSS, the coupling is worse than -25 dB between input and channels 1 and 4. As this value is comparable to the maximum gain, it jeopardizes the gain flatness and increases the oscillation risk. The effect is weaker in the two

channels further from the RF input, also because there is a ground pillar fence between them (this can be seen in Fig. 4).



(a)



(b)

Fig.9. Test results a channel in the TX MMIC (a) on the bare chip and (b) embedded in the PCB.

The coupling effect, together with a poor impedance matching, can lead to oscillations of the circuit. Thus, additional shielding methods should be utilized in the next version of the integration platform for preventing ripples and possible oscillations. Based on the reported performance, once the isolation and impedance matching are improved, the presented integration platform would overcome flip-chip over standard PCB technology [8] and would offer a performance comparable to other solutions like radio-on-glass [10] at a potentially lower cost and with higher routing and heat dissipation capabilities.

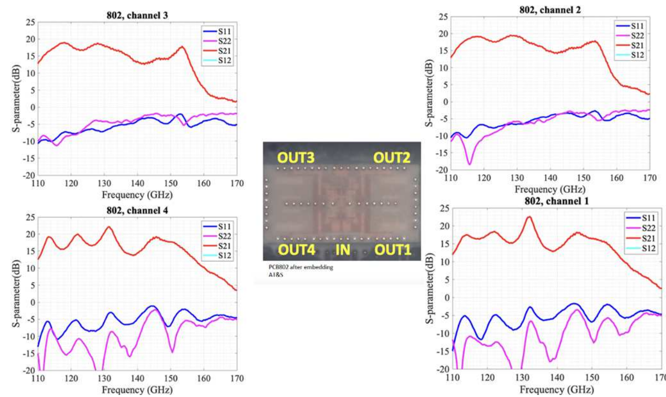


Fig. 10. Measured S-parameters for all four channels in the transmitter MMIC.

IV. CONCLUSIONS

We demonstrated key elements of an embedded component packaging platform for D-band radio systems. The embedded component packaging is highly reliable due to optimal protection of the embedded components and good heat dissipation. It increases the possible density of active and passive components. Miniaturization of the system allows keeping signal short and losses to a minimum. The testing shows promising results. However, isolation of the RF signals should be improved in the next version of the platform.

ACKNOWLEDGMENT

This work was conducted within the framework of the H2020 DRAGON project, which is partially funded by the Commission of the European Union (Grant Agreement No. 955699). We thank Mikko Kantanen for help in measuring test structures.

REFERENCES

[1] M. Jaber, M. A. Imran, R. Tafazolli and A. Tukmanov, "5G Backhaul Challenges and Emerging Research Directions: A Survey," in IEEE Access, vol. 4, pp. 1743-1766, 2016.

[2] Y. Li and J. Hansryd, "Fixed Wireless Communication Links Beyond 100 GHZ," 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, Japan, 2018, pp. 31-33.

[3] M. G. L. Frecassetti et al" D-Band Transport Solution to 5G and Beyond 5G Cellular Networks," European Conference on Networks and Communications (EuCNC), Valencia, Spain, Jun. 2019.

[4] C. Kärnfelt, B. Zhang and H. Zirath, "A QFN packaged grid array antenna in low dielectric constant LTCC for D-band applications," 2016 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP), Chengdu, 2016, pp. 1-4.

[5] A. Bisognin et al., "D-band Quasi-Yagi antenna in IPD process," 2013 7th European Conference on Antennas and Propagation (EuCAP), Gothenburg, 2013, pp. 330-331. (2015). The IEEE website, [Online]. Available: http://www.ieee.org/.

[6] H. Gulan, S. Beer, S. Diebold, P. Pahl, B. Goettel and T. Zwick, "CPW fed 2 × 2 patch array for D-band System-in-Package applications," 2012 IEEE International Workshop on Antenna Technology (iWAT), Tucson, AZ, 2012, pp. 64-67A.

[7] Lamminen, M. Lahti, D. del Rio, J. Säily, J. F. Sevillano and V. Ermolov, "Characterization of Interconnects on Multilayer High Frequency PCB for D- Band," 2020 2nd 6G Wireless Summit (6G SUMMIT), Levi, Finland, 2020, pp. 1-5, doi: 10.1109/6GSUMMIT49458.2020.9083918.

[8] D. del Rio et al., "A D-Band 16-Element Phased-Array Transceiver in 55-nm BiCMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 71, no. 2, pp. 854-869, Feb. 2023, doi: 10.1109/TMTT.2022.3203709.

[9] A. Lamminen et al., "D-Band Antenna and Array Designs for 5G Applications," 2023 Joint European Conference on Networks and Communications & 6G Summit (EuCNC/6G Summit), Gothenburg, Sweden, 2023, pp. 597-601, doi: 10.1109/EuCNC/6GSummit58263.2023.10188240.

[10] M. Elkhouly et al., "Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 76-78, doi: 10.1109/ISSCC42614.2022.973162