110 - 170 GHz 25% Duty-cycle Gilbert-cell Frequency Doubler with 6.5 dBm Peak Output Power in BiCMOS 55 nm Technology

Lorenzo Piotto, Guglielmo De Filippi, Andrea Mazzanti
Department of Electrical, Computer and Biomedical Engineering, University of Pavia, Italy

***Abstract* — Frequency multipliers are key components for signal generation above 100 GHz. Push-push frequency doublers are popular but suffer from low conversion gain and limited fundamental rejection. Mixers with quadrature inputs offer higher gain and better fundamental suppression but need a bandwidth-limiting 90° phase shifter. This work leverages Gilbert-cells mixers driven by in-phase signals but operated at a reduced duty-cycle (δ), allowing to retain the superior conversion gain and fundamental rejection without the 90° phase shifter. A simple low-frequency loop controls δ and gives maximum conversion gain by suppressing the output DC component. The signal driving the mixer switching-quad is generated and routed by a transmission-line network which compensates for the undesirable phase shift introduced by transistors parasitics, critical in the sub-THz band. Realized in SiGe BiCMOS, the circuit proves P_{out} = 6.5 dBm at 148 GHz with 7.4% power efficiency and 8 dB conversion gain. With -3 dB bandwidth of 125 - 170 GHz, P_{out} > 0 dBm from 110 to 170 GHz and a fundamental rejection always above 40 dB, the frequency doubler compares favorably against previous works.**

***Keywords* — Gilbert cell, Frequency doubler, push-push, LO generation, mm-Wave, broadband, BiCMOS.**

I. Introduction

The never-ending growth of portable, data-intensive applications needs a capacity increase of the wireless network infrastructure, driving the development of point-to-point wireless links with a 100 Gbps transfer rate in D-Band (110 - 170 GHz). Variable-frequency oscillators with low-enough phase noise cannot be implemented above 100 GHz, thus the LO signal for transceivers is generated by cascading a frequency multiplier to a lower frequency synthesizer. However, the design of power-efficient and wideband multipliers above 100 GHz is a challenging task. Frequency doublers (and in general even-order multipliers realized by cascading doublers) are preferred over odd-order multipliers giving a superior performance. Doublers can be realized with a pair of transistors in class-B (the push-push pair), which work as a full-wave rectifier when driven by anti-phase signals, but this approach has limitations [1]–[7]. The conversion gain is relatively low, and the suppression of the input signal is poor, being the circuit very sensitive to the input common-mode component. The combination of the push-push pair with injection locking techniques [1] can mitigate the above issues, but with a significant bandwidth limitation, making the approach not suitable to cover the full D-band.

Frequency doublers can also be realized leveraging a Gilbert-cell mixer in different ways, as shown in Fig. 1. In Fig. 1a, the same signal drives the Gilbert-cell at the input and LO ports. Assuming hard switching operation, the output current looks like a full rectified wave with non-zero average. The 2nd harmonic conversion gain is thus the same of the simpler push-push pair, but the Gilbert cell is ideally insensitive to the input common-mode, leading to an improved rejection of the input-frequency and odd harmonics. The current conversion efficiency can be increased by driving the input and LO port of the mixer in quadrature phase, as in Fig. 1b. In this case the output current looks like the repetition of a sinusoid chopped and flipped at half of the period, with a stronger double-frequency component. Compared to a rectified waveform, the current conversion gain is doubled [8]. However, the generation of quadrature signals needs lossy passive circuits which limit the gain advantage, are bulky and, more importantly, introduce a bandwidth limitation.

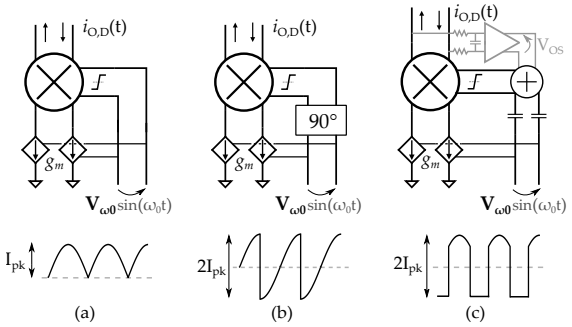


Fig. 1. Block diagrams of the Gilbert-cell based frequency doublers with in-phase driving (a), in-quadrature driving (b) and the reduced duty-cycle solution (c).

A different approach to increase the 2nd harmonic conversion gain without penalizing the bandwidth was proposed in [9]. The architecture, drawn in Fig. 1c, does not need quadrature generation and, like in Fig. 1a, the input and LO ports of the Gilbert cell are driven in phase. Here, the average value of the output is sensed, and the amplified error signal is added to the LO port as a bias voltage to suppress the DC output component by adjusting the switching duty-cycle of the mixer. The analysis in [9] proves that in steady state the mixer duty-cycle settles to around 25 % and the current conversion gain is even higher (3 dB) than that of the quadrature-driven Gilbert cell of Fig. 1b. The architecture in Fig. 1c was implemented and evaluated at a relatively low frequency, in the K band. Considering the potential for wide bandwidth with enhanced conversion gain, this paper investigates the implementation of the architecture in D-band. With the operation frequency above 100 GHz, pushed close

to the technology limit (f_{max}), the major challenge is how to manage the intrinsic phase shift introduced by device parasitic and interconnections of a non-negligible length compared to the signal wavelength. A circuit topology is presented in this paper and implemented in a 55 nm BiCMOS technology. From experimental results, the chip delivers a peak output power of 6.5 dBm at 148 GHz with 7.4 % power conversion efficiency and 8 dB of conversion gain. The -3dB bandwidth is from 125 GHz to 170 GHz and output power remains greater than 0 dBm over the full D-band, from 110 GHz to 170 GHz .

II. Circuit Description and Implementation

The schematic of the proposed frequency doubler, implementing the block diagram in Fig. 1c, is shown in Fig. 2. HBTs $Q_{1,2}$ with size of $10\,\mu m \times 0.2\,\mu m$ operate as transconductors converting the differential input voltage into a differential current $i_{IN} = i_{I,P} - i_{I,N}$. The input signal, single ended for measurement purposes, is converted to differential with an on-chip balun realized with a pair of coupled windings. The mixer switching quad is made of HBTs Q_3-Q_6, with drawn area of $6\,\mu m \times 0.2\,\mu m$. The parasitic capacitance at the output of the switching quad is resonated by inductors L_p, while a Marchand balun provides differential to single ended conversion and scales the 50 Ω off-chip termination to a 80 Ω differential load resistance for the mixer, optimal to maximize the output power. The circuit is supplied with a V_{CC} of 2 V and draws a DC current $I_{CC} = 30$ mA when driven into saturation, at an input power of 0 dBm. According to [9], as discussed in the previous section, the average (DC component) of the differential output current ($i_{O,P} - i_{O,N}$) is nulled by a low-frequency feedback loop, drawn in grey in Fig. 2, which sets a differential bias voltage (V_{OS}) to the base of Q_3-Q_6, reducing the switching-quad duty-cycle. The differential DC component is sensed by resistors $R_{sense} = 5.5\,\Omega$ in series with inductors L_p. To not impair the quality factor of the load resonator, and avoid performance penalty, R_{sense} are shunted by capacitors $C_{big} = 1.5$ pF., large enough to be considered a short circuit in D-band. The error voltage across the sense resistors is amplified by a fully differential OTA. The output voltage of the OTA, V_{OS}, biases the bases of the switching quad via resistors $R_{big} = 1\,k\Omega$. The OTA is made of two gain stages allowing to reach a low frequency loop gain of 40 dB. The stability is ensured by Miller compensation which also limits the loop bandwidth to 200 MHz. The OTA draws 250 μA from the 2 V supply. The overall power consumption of the low frequency biasing loop is 3 mW (500 μW consumed by the OTA and 2.5 mW due to the 80 mV DC drop across R_{sense}) and represents only 5 % of the overall doubler power consumption.

For maximum 2nd harmonic conversion gain, the current entering the common emitter node of the switching quad ($i_{I2,P} - i_{I2,P}$) must be in phase with the voltage driving the base of Q_3-Q_6 (V_{LO} in Fig. 2). At operation frequency far below the transistors cut-off frequency, as in [9], this condition is achieved by feeding the base of Q_3-Q_6 with the same voltage that drives the common emitter transconductors, Q_1, Q_2. As frequency approaches the technology f_t/f_{max}, this

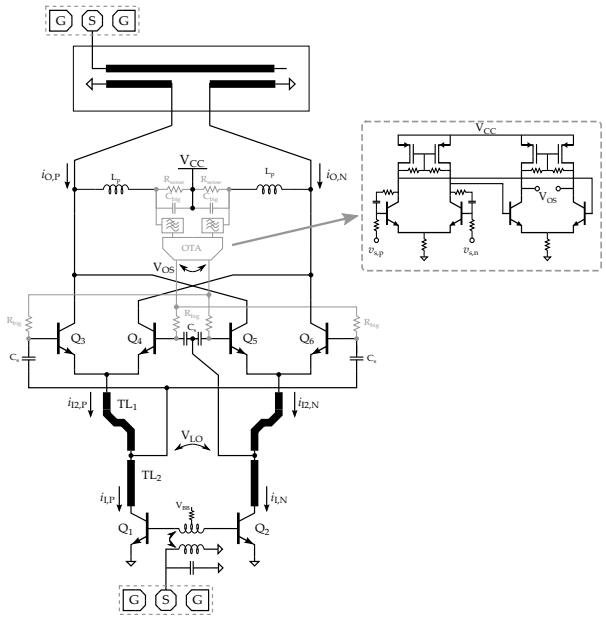


Fig. 2. Schematic of the proposed frequency doubler.

straightforward implementation is no longer viable, because of the non-negligible phase shift introduced by transistors parasitic and the delay of interconnections. As an example, the extrinsic HBTs base resistance, r_{bb}, forms a low-pass filter with the base-to-emitter capacitance, c_π, with an associated pole at about 140 GHz in the adopted technology. With a 75 GHz frequency of the input signal, the pole delays the effective voltage at the internal base of Q_3-Q_6 by roughly 30°. Moreover, while at low frequency the common-emitter transconductors are connected directly to the switching quad, the output resistance of Q_1, Q_2 at high frequency is drastically reduced, suggesting the introduction of an interstage matching network to rise the signal injection into the switching quad and increase the conversion gain. Looking again at Fig. 2, in the proposed frequency doubler the current provided by Q_1, Q_2 is injected into the switching quad through a transmission line (TL_1+TL_2) and the voltage V_{LO} that drives the base of Q_3-Q_6 is extracted from an intermediate tap. The first section of the line, TL_1, has a dual purpose: first, together with the stray capacitances of Q_3-Q_6, TL_1 provides step-up transformation of the impedance at the emitters of the switching quad, rising the amplitude of the voltage V_{LO} thus leading to a better current commutation of the switching quad. Second, TL_1 compensates the phase shift introduced by parasitics of Q_3-Q_6 by introducing a delay between the current which is finally entering into the switching quad and V_{LO}. To gain insight, Fig. 3 plots the current conversion gain $\left(CG = \frac{(i_{O,P} - i_{O,N})|_{2fin}}{i_{I2,P} - i_{I2,N}}\right)$, the amplitude of V_{LO} and the bias voltage produced by the OTA, V_{OS}, versus the length of TL_1 (L_{TL1}) when the multiplier is driven at 0 dBm input power. The amplitude of V_{LO} rises with the length of TL_1, reaching the maximum of 600 mV for $L_{TL1} = 150\,\mu m$. On the other hand, the CG peaks to -2 dB at $L_{TL1} = 75\,\mu m$, when

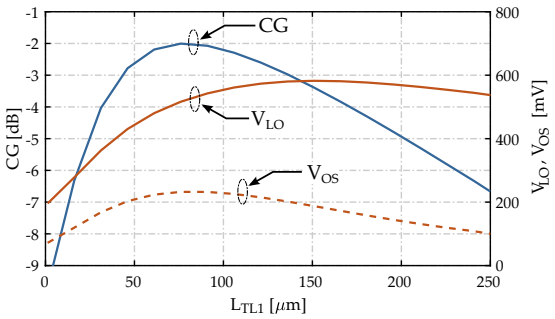


Fig. 3. Frequency doubler conversion gain versus TL_1 length.

the phase delay is optimally compensated, despite a V_{LO} slightly below its maximum. The bias voltage V_{OS} is also maximized for $L_{TL1} = 75\,\mu$m, confirming that, at this length of TL_1, the duty-cycle of the switching quad is minimized [9]. TL_2 provides conjugate matching to the output impedance of Q_1, Q_2 further increasing the conversion gain. Fig. 4 plots the same quantities of Fig. 3 versus the length of TL_2 (L_{TL2}). V_{LO} rises close to 1 V and the $\left(CG = \frac{(i_{O,P} - i_{O,N})|_{2fin}}{i_{I,P} - i_{I,N}}\right)$ increases from -2 dB to roughly 0 dB at $L_{TL2} = 300\,\mu$m.

Tlines TL_1 and TL_2 are realized as a shielded coplanar structure with the signal in the topmost metal (M9) and the coplanar ground on the second topmost metal (M8). The characteristic impedance is 65 Ω with a quality factor ≈ 25. TL_1 and TL_2 are also easily laid without additional interconnections that would add parasitic elements in D-band. The frequency doubler is realized in STM BiCMOS 55 nm technology. The chip photograph is reported in Fig. 5a, with core area 390 x 250 μm^2 excluding GSG pads. Not considering input and output baluns, only required for measurements, the area of the frequency doubler is 200 x 140 μm^2. The layout of half of the core is highlighted in Fig. 5b. TL_2 is folded on top of Q_1,Q_2 while TL_1 is wrapped around the switching quad, allowing a straight connection to the base and emitter terminals of Q_3-Q_6.

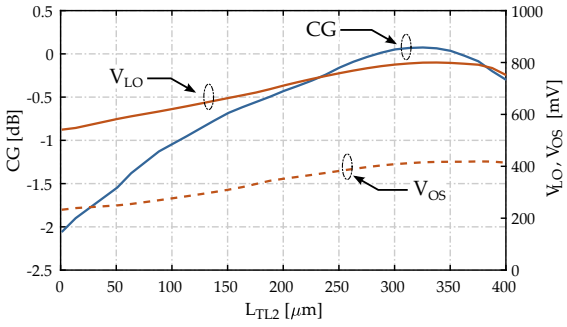
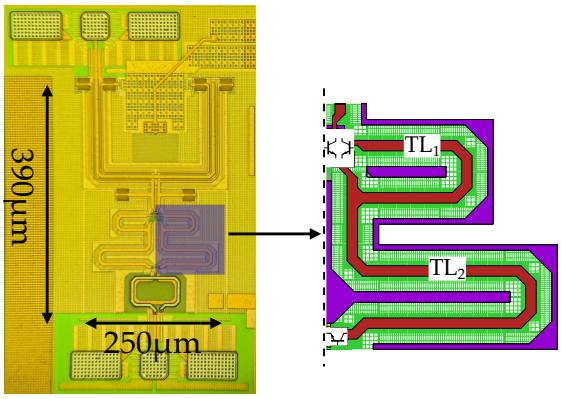


Fig. 4. Frequency doubler conversion gain versus TL_2 length.

III. Experimental Results

The chip was measured with direct die probing. The input signal is provided by an Agilent E8257D signal generator to cover the 50 - 67 GHz band and with an OML N5256BW12 frequency extension module for the 67 - 85 GHz band. Output power at twice the input frequency is measured with an



(a) (b)

Fig. 5. Photograph of the realized frequency doubler (a) and layout of half of the core (b).

ELVA-1 DPM-06 D-band power meter, while the fundamental leakage component is characterized with harmonic mixers and a PXA N9030A spectrum analyzer.

Fig. 6 shows the measured and simulated output power, P_{sat}, and collector efficiency ($\eta = P_{sat}/P_{DC}$). P_{sat} peaks to 6.5 dBm at 148 GHz and remains within -3 dB from 125 GHz to at least 170 GHz, the upper limit of the measurement setup, corresponding to a fractional bandwidth larger than of 31%. P_{sat} is above 0 dBm over the full D-band [110 - 170] GHz. Measurements are well aligned with simulations, which predict a 3 dB bandwidth of [125 - 175] GHz and a remarkable $P_{sat} > 0$ dBm bandwidth [110 - 200] GHz, corresponding to a 60% fractional bandwidth. Fig. 7 shows the 2nd harmonic conversion gain (CG), η and output power (P_{out}) at input frequency of 150 GHz versus the input power (P_{in}). The CG peaks to 8.5 dB at $P_{in} = -4$ dBm. With $P_{in} = 0$ dBm, used for the measurements in Fig. 6, the conversion gain penalty is <1 dB.

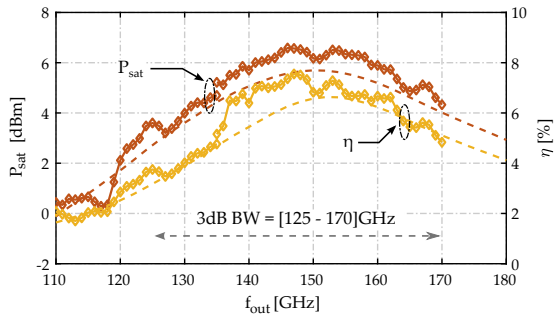


Fig. 6. Measured (solid) and simulated (dashed) output saturated power (P_{sat}), and collector efficiency (η) vs frequency.

The fundamental rejection of the input signal is measured at $P_{in} = 0$ dBm. The unavoidable coupling between input and output probes has been characterized and de-embedded from the measurement. Results are reported in Fig. 8, showing a fundamental rejection above 40 dB over the entire bandwidth. The measured results are finally summarized in Table 1 and compared against previously reported frequency doublers operating in a similar frequency range. The implemented frequency doubler displays high P_{sat} and CG simultaneously

Table 1. Performance summary and comparison table.

	This Work	[1]	[2]	[3]	[4]	[5]	[6]	[10]	[7]
Technology	55 nm SiGe	55 nm SiGe	0.13 μm SiGe	90 nm SiGe	0.13 μm SiGe	22 nm FDSOI	55 nm CMOS	0.1 μm GaAs	InGaAs
Architecture	Reduced-δ Gilbert-cell	Push-Push	Push-Push	Push-Push	Push-Push	Push-Push	Push-Push	Common Source	Push-Push
Frequency [GHz]	125 - 170	116 - 144	138 - 170	128 - 140	166 - 182	125 - 145	112 - 125	110 - 130	100 - 208
BW [%]	31	22	21	9	9	15	11	17	75
P_{sat} [dBm]	6.5	4.3	5.6	9.4	4.5	4.1	7.8	5	1.4
CG@P_{sat} [dB]	8	9.3	4.9	-6	5	-7.6	-2.2	2	-12.6
η [%]	7.4	7.2	10.1	12.1	8.4	10.4	6.8	4.9	9.6
PAE@P_{sat} [%]	6.3	6.4	6.8	<0	5.8	<0	<0	1.8	<0
Fund. Rejection [dB]	>40	>32	37	20	-	15	20	25	-
P_{DC}/V_{CC} [mW/V]	60 / 2	37.4 / 2	36 / 1.5	72 / 1.9	33.5 / 2.5	24.7 / 0.8	88 / 1.2	65 / 1	14.4 / 0.8

and the highest rejection of the fundamental signal. The -3 dB fractional bandwidth of 31% is also the largest reported in a silicon-based technology. [7], in a compound semiconductor technology, demonstrates a wider bandwidth but with significantly lower P_{sat} and a high conversion loss.

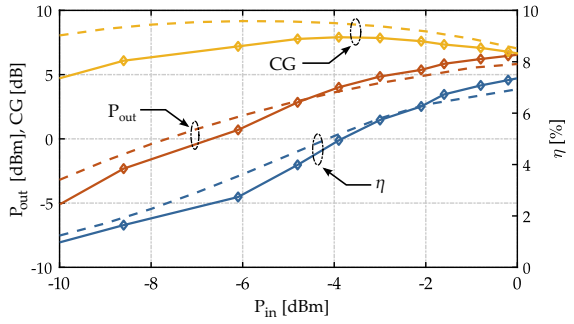


Fig. 7. Measured output power (P_{out}), Conversion Gain (CG) and collector efficiency (η) vs input power P_{in} @ f_{out} = 150 GHz.

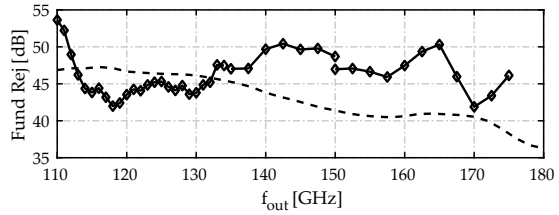


Fig. 8. Measured (solid) and post-layout simulated (dashed) fundamental harmonic rejection vs frequency.

IV. Conclusion

A mixer-based frequency doubler in D-band has been presented. The two ports of the mixer are driven by signal in-phase and a feedback loop cancels the DC offset and boosts the conversion gain by reducing the switching-quad duty-cycle. A band-limited quadrature phase shifter is avoided, leading to wideband operation. A transmission line network that compensates the phase shift introduced by transistors parasitic is proposed to generate the LO signal and drive the mixer optimally. The advantages are proved by experiments on a test chip in 55 nm SiGe BiCMOS. Compared to previous works, the doubler displays the widest operation bandwidth and the highest suppression of the fundamental component with high P_{sat} and conversion gain, simultaneously.

Acknowledgment

This work received funding from the Commission of the European Union within the H2020 DRAGON project (Grant Agreement No. 955699) and KDT SHIFT project (Grant Agreement No. 1010962).

References

[1] M. M. Pirbazari and A. Mazzanti, "High Gain 130-GHz Frequency Doubler with Colpitts Output Buffer Delivering Pout up to 8 dBm with 6% PAE in 55-nm SiGe BiCMOS," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 36–39, 2021.

[2] C. Coen, S. Zeinolabedinzadeh, M. Kaynak, B. Tillack, and J. D. Cressler, "A highly-efficient 138–170 GHz SiGe HBT frequency doubler for power-constrained applications," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2016, pp. 23–26.

[3] S. G. Rao, M. Frounchi, and J. D. Cressler, "Triaxial Balun With Inherent Harmonic Reflection for Millimeter-Wave Frequency Doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2822–2831, 2021.

[4] Y. Li, W. L. Goh, and Y.-Z. Xiong, "A Frequency Doubler/Modulator With 4.5 dBm Output Power at 170 GHz Using SiGe HBTs," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 3, pp. 181–183, 2015.

[5] M. Mock, I. K. Aksoyak, and A. C. Ulusoy, "A High-Efficiency D-Band Frequency Doubler in 22-nm FDSOI CMOS," in *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 272–275.

[6] Z. Yang, K. Ma, F. Meng, and B. Liu, "A 120-GHz Class-F Frequency Doubler with 7.8-dBm Pout in 55-nm Bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 8, pp. 2173–2188, 2023.

[7] U. J. Lewark, S. Diebold, S. Wagner, A. Tessmann, A. Leuther, T. Zwick, and I. Kallfass, "A Miniaturized Unit Cell for Ultra-Broadband Active Millimeter-Wave Frequency Multiplication," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1343–1351, 2014.

[8] M. Frounchi, S. G. Rao, and J. D. Cressler, "A *ka*-Band SiGe Bootstrapped Gilbert Frequency Doubler with 26.2% PAE," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 12, pp. 1122–1124, 2018.

[9] L. Piotto, G. D. Filippi, G. Brozzetti, D. D. Maistro, S. Erba, and A. Mazzanti, "A 14–32 GHz SiGe-BiCMOS Gilbert-Cell Frequency Doubler With Self-Adjusted Reduced Duty-Cycle Performance Enhancement," *IEEE Journal of Solid-State Circuits*, pp. 1–11, 2023.

[10] M. Abbasi, R. Kozhuharov, C. Karnfelt, I. Angelov, I. Kallfass, A. Leuther, and H. Zirath, "Single-Chip Frequency Multiplier Chains for Millimeter-Wave Signal Generation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3134–3142, 2009.