D-band Stacked Common-Base Power Amplifier with 19.2 dBm oP_{1dB} in 55 nm SiGe BiCMOS

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***Abstract*—This paper presents the design and experimental validation of a stacked common-base power amplifier (PA) tailored for D-band communication systems. Leveraging 55 nm SiGe BiCMOS technology, the proposed PA architecture combines the superior gain compression performance of the common-base topology with the higher voltage swing provided by stacked-transistor power amplifiers. Experimental results demonstrate a peak output power of 19.7 dBm with only a 0.5 dB lower 1-dB compression point (oP_{1dB}) of 19.2 dBm at 135 GHz. The power added efficiency (PAE) reaches 12.1 % at saturation and 11.5 % at oP_{1dB}.**

***Index Terms*—BiCMOS, D-band, millimeter-wave, power amplifier (PA), common base (CB), current clamping, stacking power amplifier.**

I. Introduction

The D-band has garnered significant interest in recent years due to its potential for next-generation communication links with speeds reaching tens of gigabits per second. To attain high data rates, it is essential to utilize advanced modulation techniques capable of transmitting a greater number of bits per symbol. However, as modulation schemes become more sophisticated, they impose more stringent performance requirements on transceivers. Power amplifiers (PAs) are crucial components since they exhibit gain compression behavior, hindering accurate transmission of symbols at the constellation's extremities and thereby affecting transmission quality. Addressing this issue involves operating PAs in regions below the oP_{1dB}. Nonetheless, PA efficiency typically peaks near the saturation power (P_{sat}), sharply declining with decreasing output power. This poses a significant challenge, particularly in the D-band, where efficiency peaks around 10-15%, and drops to just a few percentage points in backoff conditions. Consequently, achieving high-order modulation schemes forces PAs to operate in highly inefficient regions. In single-channel transceivers adopted at lower frequencies, digital predistortion techniques can effectively mitigate gain compression. However, D-band transceivers often feature multiple channels to integrate phased array systems with beamsteering functionality [1]. Attempting to implement digital predistortion across each channel of the array would be impractical and inefficient.

Cascode-based output stages are widely adopted in D-band amplifiers, with P_{sat} as high as 22.7 dBm [2]. However, they suffer from soft saturation, with oP_{1dB} lower than 18 dBm. Among the analyzed works, all cascode-based amplifiers exhibit a P_{sat}/oP_{1dB} gap of 2.4 dB at best, but more frequently, it aligns to values of 3 or 4 dB [2]–[5]. On contrary, PAs based on common-base (CB) output stages have proven to provide a <1 dB P_{sat}/oP_{1dB} gap, with PAE in line or better than

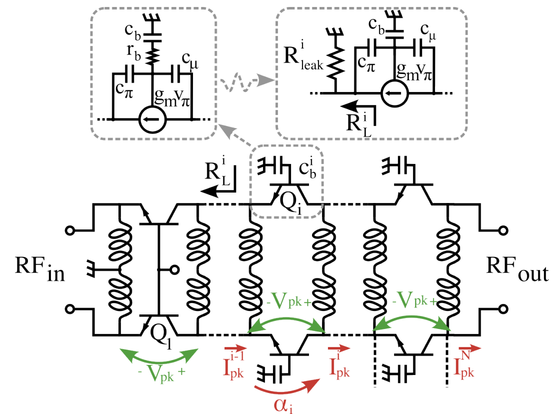

Fig. 1. Schematic depicting the working principle of a stacked power amplifier.

cascode-based PAs [6]. Furthermore, CB stages easily implement dynamic biasing through current clamping techniques, which significantly improve backoff PAE. However, P_{sat} is limited by the maximum voltage swing that a single transistor can sustain.

To capitalize on the superior gain compression performance of the CB configuration while augmenting the output voltage, a viable approach entails employing device stacking to uniformly distribute voltage stress across the transistors [7]. Despite its widespread adoption at lower frequencies, investigation and application within the D-band spectrum remain largely unexplored.

This work examines the advantages of integrating transistor stacking techniques, addressing challenges encountered when the operating frequency of the transistor approaches its ft/fmax. An optimal trade-off between output power and efficiency is found to be achieved with a two-stacked stage configuration, while the utilization of CB input stages for oP_{1dB} improvement is also explored. Additionally, a load impedance sizing technique, which considers transistor current losses, is introduced. The final design is composed of two power amplifier units combined by means of a Marchand balun-based power combiner.

II. Output Stage Design

The schematic principle of an N-transistor stacking amplifier is shown in Fig. 1. Assuming the impedance at the emitter of each transistor is real, since the same current flows through all the devices in the stack, each transistor has to load the preceding one with an impedance $R^i{}_L = \frac{i-1}{N} R_L$. This result is usually achieved by means of capacitive loading of the base

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[7]. The network created by the explicit base capacitance C_b, the parasitic base-emitter capacitance C_π, and the parasitic base-collector capacitance C_μ acts as a weighted summer between the input and output voltage of the devices. The resulting base-emitter voltage controls the transconductance. With this technique, the CB input impedance $R^i{}_L$ is raised from its original $1/g_m$ to the targeted $\frac{i-1}{N}R_L$.

This technique is popular at frequencies below 50 GHz, where the model can be further simplified by ignoring the presence of C_μ. As the frequency increases, the impact of the capacitances' reactance becomes a major issue. First, part of the signal current does not exit the transistor but is drawn by the parasitic elements. Second, it creates a misalignment of the voltage phases, limiting the output voltage swing. To compensate for this behavior, the parallel inductors shown in Fig.1 are necessary at the input and output of the stages to resonate with the capacitance elements [8].

If all of the reactive components are resonated, and each stage of the circuit shows the proper impedance to the previous one, all the current at the input is expected to flow to the output, while the voltage stress is equally distributed along the stacked transistors, resulting in an output power benefit of $20\log_{10}N$. Unfortunately, circuit inspection reveals that part of the signal current is spilled out of the circuit at each stacking step. The ratio between the input and output current of each stage can be identified with a current gain α_i, which is always lower than one.

The main cause of this current leak is attributed to the transistor base resistance r_b. As the operating frequency of the circuit increases, the quality factor of the parasitic capacitances decreases as the value of the base resistance becomes comparable with the reactances of C_π, C_μ, and C_b. Its impact can be synthesized as a parallel resistance $R^i{}_{leak}$ at the input of each stage, which sinks a portion of the signal current. Then, α_i is computed as the attenuation of the current divider created by $R^i{}_{leak}$ and $R^i{}_L$.

$$R^i{}_{leak} \sim \frac{(c_b + c_\mu + c_\pi)^2}{c_b{}^2 c_\pi\,(c_\mu + c_\pi)\,r_b \omega^2}, \quad \alpha_i \sim \frac{1}{1 + R^i{}_L/R^i{}_{leak}}$$

Since all the stacked transistors are in series, the overall current gain (α_{tot}) of the amplifier is the product of the individual current gains of each transistor ($\prod_{i=1}^{N}\alpha_i$). As only a fraction α_{tot} of the input current reaches the output, both output power and collector efficiency are penalized by a factor of $1/\alpha_{\text{tot}}{}^2$. This comes from the fact that the impedances were designed assuming $\alpha_{\text{tot}} = 1$, but the signal current decreases along the path due to losses. Consequently, the collector-emitter voltages developed on the transistors are lower than expected, resulting in a reduction in voltage efficiency as well.

While little can be done to bring the value of α_i of each stage closer to unity, the transistor collector-emitter voltage distribution can be restored by scaling each stage's input impedance by a factor of $1/\prod_{j=1}^{i-1}\alpha_j$. Fig. 2 illustrates the expected output power from a stacked power amplifier with three different configurations.

If the stacking is lossless, the output power grows by a factor of $10\log_2 N$. Considering the base resistance of the device, the output power is penalyzed by 2 dB and 5 dB, respectively, with the two- and three-stacked transistor configurations. Conversely, impedance equalization allows limiting the output power penalty to only 1 dB in the case of two stacked transistors, while it performs worse for higher stacking levels. The higher output power obtained in the two-stacked transistor case with equalized impedances also leads to a significant improvement in collector efficiency over a standard design, with a 3 % increase resulting from the higher voltage efficiency.

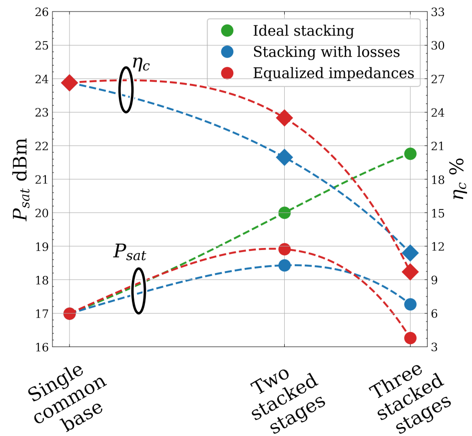

Fig. 2. Simulated P_{sat} and collector efficiency (η_c) of single, double and triple stacked CB PA.

III. Circuit Design

The schematic of the complete circuit is shown in Fig. 3. In the output stage, the lower pair of transistors Q_{2a-b} are arranged in a CB fashion, while the upper pair Q_{1a-b} are loaded at their base terminals with capacitances C_{1a-b}. The optimum load $R^I{}_L$ for the CB transistors is found to be approximately 45 Ω. Consequently, to develop the same collector emitter voltage swing on both transistors Q_{1a-b} and Q_{2a-b}, the stacked transistor load $R^{II}{}_L$ should be set to twice the value of $R^I{}_L$, thus 90 Ω. However, as previously mentioned, the stacking transistor current gain η_i in this frequency range is assessed to be around ∼0.68. In the proposed design, $R^{II}{}_L$ is scaled up by a factor of $1/\eta_i$ to 132 Ω. The output current is similar to the previous case, but the output voltage swing is restored, resulting in $V_{ce}{}^{Q_{1a-d}}$ being equal in amplitude to $V_{ce}{}^{Q_{2a-d}}$ and an output power 1.2 dB greater than the case where impedance scaling is not performed. With a voltage supply of 3.7 V and considering a peak voltage swing of 3.2 V, approximately 15.9 dBm of output power is expected to be produced by each branch of the output stage. The values of C_{1a-b} are chosen to load Q_{2a-b} with the targeted real impedance $R^I{}_{leak}$, while two pairs of coplanar transmission lines TL_{2a-b} and TL_{1a-b} are implemented to resonate the imaginary part of the impedances, respectively, at the output of the CB and of the power amplifier. To enhance backoff PAE, CB stages employ current clamping behavior to track the signal current with the transistor DC current [6]. As the input current increases, transistors Q_{2a-d} turn off, causing the shunted transmission lines TL_{3a-b} to charge. Once the

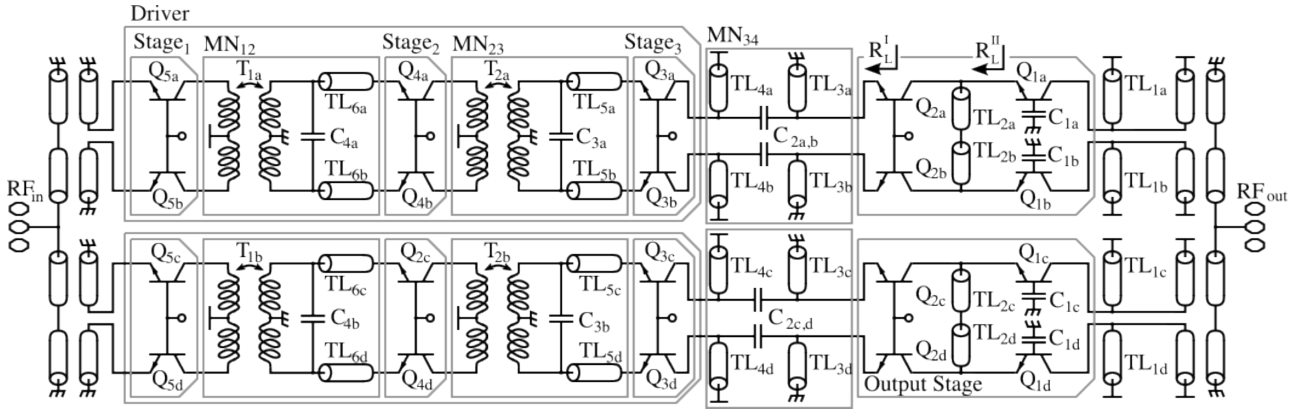

Fig. 3. Complete schematic of the proposed power amplifier.

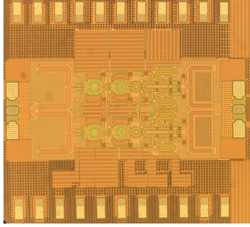
Fig. 4. Chip microphotograph. (Die size is 1250 $\mu m \times 500\,\mu m$).

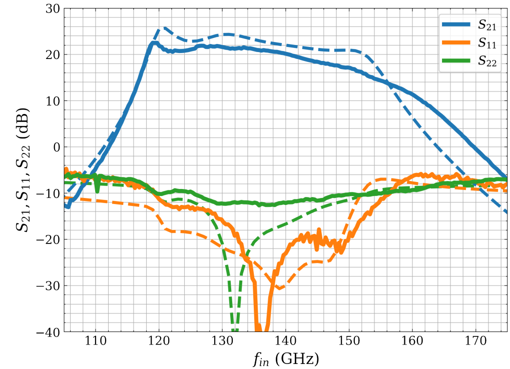

Fig. 5. Power amplifier simulated (dashed lines) and measured (continuous lines) S-parameters.

average current on TL_{3a-b} equals the peak signal current, Q_{2a-d} turn back on. The duration of the period when the transistor is off is negligible compared to the modulated signal time constants, ensuring minimal impact [9].

The output stage is forerun by a three stages driver circuit forming a power amplifier units. Two of this units are placed in parallel while two passive structures act respectively as power splitter at the input and as power combiner at the output. Each of this structures perform a single-ended to two paths differential conversion and it is implemented with two $\lambda/4$ coplanar coupled transmission lines Marchand balun whose single-ended side is in parallel.

The three-stage driver is based on a differential CB topology. Transistor area scales proportionally with the power each stage handles, starting at 0.9 μm^2 for Q_{5a-b}, then increasing to 1.8 μm^2 for Q_{4a-b} and 3.9 μm^2 for Q_{3a-b}. Intrastage matching networks between the driver stages are implemented using a combination of distributed and lumped passive elements. Given the G_p of the output stage is less than 5 dB, the driver has to deliver high power to preserve the PA's oP_{1dB}. Consequently, its power consumption significantly impacts the overall efficiency of the PA. To address this, a current clamping technique is also applied to this stage, albeit with a less aggressive current expansion factor compared to the output stage.

IV. Experimental Results

The proposed D-band power amplifier was implemented in STMicroelectronics 55 nm BiCMOS. The chip micrograph is shown in Fig. 4. The silicon area occupied by the design is 0.65 mm^2, including the pads. Measurements were carried out by wafer probing for high-frequency signals, while the supply and biasing pads were wire bonded to a carrier PCB.

The measured S-parameters of the power amplifier are shown in Fig. 5. A comparison between the measured and simulated S_{21} highlights an underestimation of the matching network insertion losses, resulting in higher gain in the upper part of the frequency range. However, the peak measured S_{21} reached 22.5,dB at 125,GHz, decreasing at higher frequencies.

Continuous wave (CW) performance of the PA at the central frequency of 135 GHz is reported in Fig. 6. The PA exhibits a P_sat of 19.7 dBm and an oP_{1dB} of 19.2 dBm. The PAE peaks at 12.1 % corresponding to P_sat. Since the $\text{P}_\text{sat}/oP_{\text{1dB}}$ gap is limited to 0.5 dB, at oP_{1dB}, the PA maintains a PAE of 11.5 %, close to the value achieved at P_sat. The measured power gain of the PA is 22.5 dB, in agreement with S-parameters measurements.

Fig. 7 illustrates the DC current behavior of the different stages of the PA in response to input power. Two supply voltages are used: 3.7 V for the output stage and 1.8 V for the three stages of the driver. As described in Section III, all stages of the PA employ the current-clamping technique to adjust the DC current according to the output power. The output stage has a DC current of 139 mA at P_sat. In the absence of current clamping, a standard class-A design consumes the same current even at 6 dB backoff from P_sat. However, with current clamping this current is reduced to 72 mA. If current clamping is extended to the driver stages, it results in ∼40 % reduction of the driver current, from 90 mA at P_sat to 55 mA at 6 dB backoff. The DC current modulation exploiting current clamping in both the output stage and the driver improves the backoff PAE from 3.1 % of a conventional Class A biasing to 5.7 %.

Gain compression measurements at different frequencies in the D-band range have been carried out. The main results are reported in Fig. 8. The power gain profile is similar to

TABLE I
PERFORMANCE COMPARISON

	This Work	[6]	[10]	[3]	[5]	[4]	[2]	[11]
Technology node	BiCMOS 55 nm	BiCMOS 55 nm	SiGe 90 nm	SiGe 130 nm	SiGe 130 nm	SiGe 90 nm	Sige 130 nm	BiCMOS 130 nm
Topology	CB/CB	CB	CE	CE/CC	CE/CC	CE/CC	CE/CC	CE/CC
f_o (GHz)	135.0	135.0	116.0	130.0	121.0	127.5	161.0	160.0
BW_{3dB} (GHz)	37.0	34.0	12.0	30.0	28.0	35.0	40.0	20.0
G_p (dB)	22.5	24.0	15.0	34.0	21.8	18.2	30.7	24.0
P_{sat} (dBm)	19.7	17.6	20.8	17.0	22.7	21.9	18.1	18.0
$PAE@P_{sat}$ %	12.1	17.5	7.6	13.0	18.7	12.5	12.4	9.4
oP_{1dB} (dBm)	19.2	16.8	17.0	14.6	18.0	18.6	14.0	15.0
$PAE@oP_{1dB}$ %	11.5	17.1	4.5[1]	9.0[1]	9.8[1]	9.0[1]	7.5[1]	5.0[1]

[1] Graphically extrapolated.

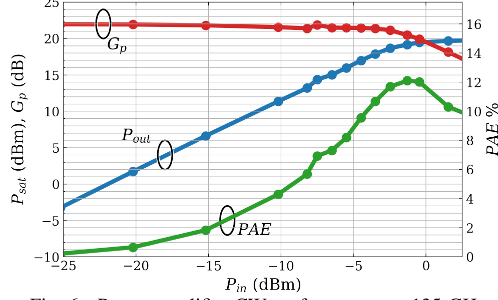

Fig. 6. Power amplifier CW performances at 135 GHz.

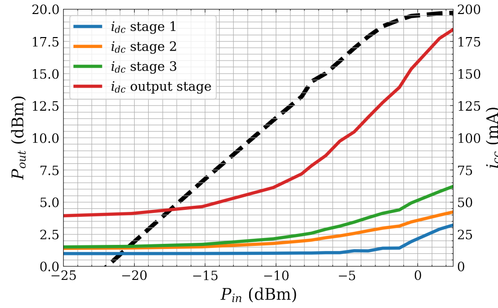

Fig. 7. DC current expansion of the different stages of the PA versus P_{in}.

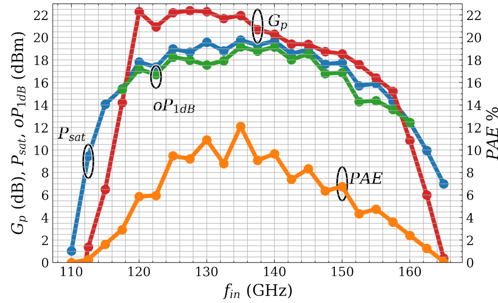

Fig. 8. Power amplifier measured G_p, P_{sat}, oP_{1dB} and PAE over the spectrum.

the result predicted by the S-parameters, with a peak gain of 22 dB achieved at 125 GHz. The P_{sat} characteristic is centered at 135 GHz. The oP_{1dB} follows the P_{sat} over the operating bandwidth with the 0.5 dB gap previously highlighted.

The main PA performances are summarized in Table I and compared with state of the art SiGe and BiCMOS D-band PAs with $P_{sat} > 15$ dBm. Despite the higher P_{sat} of similar works, the proposed PA results in the largest oP_{1dB} because of the minimum P_{sat}/oP_{1dB} gap. PAE at P_{sat} is in line with the literature but is the highest among PA with $P_{sat} > 19$ dBm at the oP_{1dB}.

V. CONCLUSION

The paper presented a stacked common base D-band power amplifier in a 55 nm SiGe BiCMOS technology. Circuit analysis accounting for the loss of HBTs has proved that there is no advantage by stacking more than two transistors and the performance can be optimized by equalizing the impedence levels in the stack. Experimental results demonstrated oP_{1dB} of 19.2 dBm, only 0.5 dB lower than the P_{sat} of 19.7 dBm at 135 GHz. The PAEs at P_{sat} and oP_{1dB} are 12.1 % and 11.5 %, respectively. Using transistors in common-base and by exploiting the current clamping technique across all stages of the PA, power consumption is modulated from 216 mW at the quiescent point to 676 mW at P_{sat}.

VI. ACKNOWLEDGMENT

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